

A High Frequency Time Domain Measurement System and its Application to Robust and Scientific Ultra-Wide Band MMIC design for Military Applications

T.V. Williams¹, D. FitzPatrick¹, M. Haynes², C. Whittle², J. Benedikt¹ and P. J. Tasker¹

¹Cardiff University, Queens Buildings,
The Parade, Cardiff, CF24 3AA

²SELEX Sensors and Airborne Systems Limited, 300 Capability Green,
Luton, Bedfordshire, LU1 3PG

Abstract

Significant challenges persist to date in the field of high frequency MMIC design, with the majority of designs based upon rather simplistic approximations or device models. The development of such models requires significant time and cost investment. This means that their application tends to be limited to very specific operating conditions limiting the permitted design space. This situation often leads to differences between simulated and measured circuit performance resulting in iterative design improvements requiring multiple wafer runs to meet the desired specifications. This paper presents an approach that can allow mitigation of the device modelling issue by exploiting a novel measurement system, operating at high frequencies up to 40 GHz to provide measured and engineered large signal time domain voltage and current waveforms at the device plane that can be directly imported into commercial CAD software. The resulting measurement-based device models are available immediately after the conclusion of measurements enabling a very rapid and robust design approach.

Keywords: Active Load-pull, MMIC Design, PA's

Introduction

o a simulation environment. However for such an approach to be useful the device models employed must be very accurate and robust. The difficulty in achieving this becomes apparent when we consider that non-linear devices are very complex and react to a significant number of variables such as bias, RF power level, temperature and impedance environment. Considerable effort has been made to derive behavioural, physical or equivalent circuit based models that produce accurate predictions of large signal performance under all operating conditions. This however, is an extremely time consuming process which often leads to the permitted design space being bound to a limited number of operating conditions.

Ideally all activity in the field of high frequency design should be confined t

The alternative approach employed in this paper is to use measured data under varying operating conditions directly in the design process. This approach is facilitated through a direct waveform look-up model [1] employed within a commercially available simulation environment (Agilent ADS) allowing the measured voltage and current waveforms to be used during simulation, allowing for a more robust and scientifically based design solution. Further work is ongoing in this area that has the potential to dramatically reduce measurement time and allow for a more simplistic integration into CAD [5].

This measurement based design approach has previously been successfully

demonstrated in the optimisation of narrow band power amplifier (PA) architectures for the communications sector [2-4], showing the strong potential of such an approach.

To allow this robust design approach to be applied to military applications it was necessary to design, configure, calibrate and verify a new large signal device characterisation system that allows control of all of the relevant variables. The realisation of this new high frequency waveform measurement system is discussed in this paper along with the steps taken to validate the operation of the new system. Once the measurement system had been fully validated a number of measurement activities were conducted. One example is presented here where a 6x100µm device is fully characterised over a wide bandwidth of 5-10 GHz. This characterisation highlights that the measured data can in fact be used in both directions allowing feedback to the device manufacturer of device related issues and feedback to the circuit designer providing the optimal environment and operating conditions to get the maximum performance out of the device.

Finally the first excitation of the full design loop will be discussed where the measured data was used by SELEX S&S to optimise the matching design of a 6 x 100µm driver amplifier. Results achieved were dramatically different when compared to a more traditional inter-stage circuit optimisation approach.

Measurement System Realisation

A photograph of the realised measurement system is shown in figure 1, with a block diagram shown in figure 2. The system uses two broad-band directional couplers to simultaneously measure all four incident (a) and reflected (b) waves, a computer controlled DC source is used, as the DC cannot be measured via the couplers. This allows construction of the full waveforms in software by simply adding the DC

voltage and current information into the measured RF waveforms. The system is fully vector corrected allowing absolute measurement of the RF travelling waves at the device plane. This means that in addition to simple s-parameter type measurements the system can also be used to collect fully corrected large signal input and output voltage and current waveforms at the device plane. Knowledge of the system impedance environment allows the voltage and current waveforms to be simply determined from the vector error corrected incident (a_n) and reflected (b_n) travelling waves using equations (1) and (2) :

$$v_n = \sqrt{Z_0} \cdot (a_n + b_n) \quad (1)$$

$$i_n = (a_n - b_n) / \sqrt{Z_0} \quad (2)$$

If desired the captured waveforms can be processed in software¹ to provide magnitude and phase information at each constituent frequency.

The frequency response of the RF couplers and the sampling heads of the oscilloscope define the bandwidth of the measurement system. The system built uses 1-40 GHz directional couplers and 60GHz sample heads (3dB bandwidth).



Figure 1 – Photograph of the realised Measurement System

A major difficulty with using a sampling oscilloscope is the requirement for a separate trigger signal, often at much lower frequency than the stimulus signal, for example in the case of the Tektronix DSA

¹ IGOR Pro, Wavemetrics Inc.

the maximum trigger frequency is 12.5 GHz, whereas measurements were required with stimulus frequencies up to 40 GHz. To ensure measurement accuracy it is imperative that absolute phase coherence is

maintained between the trigger signal and the measured signals, therefore a novel triggering architecture was devised.

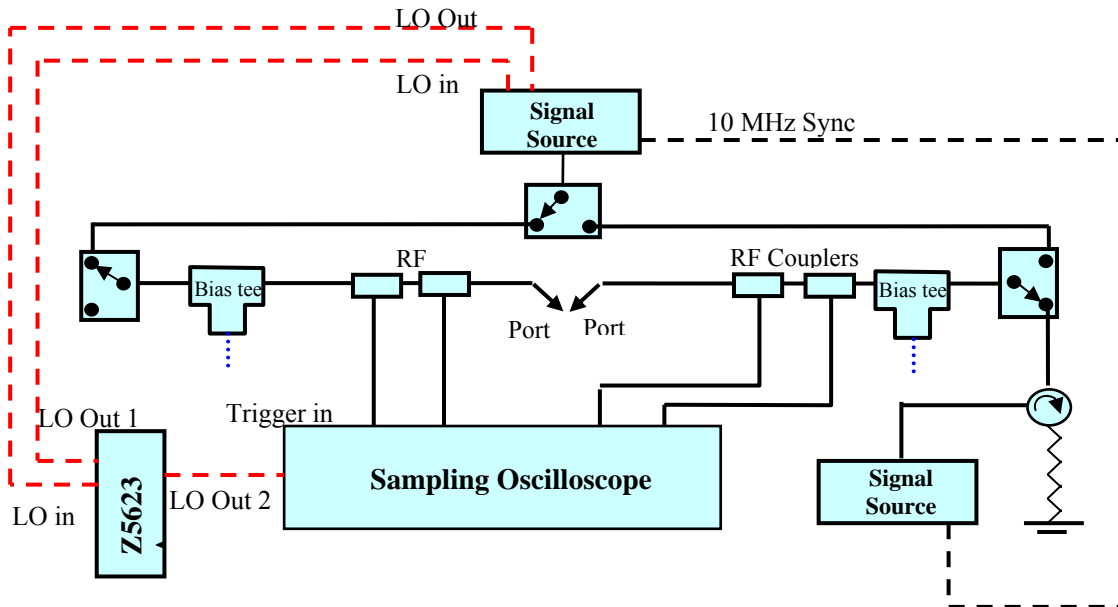


Figure 2 – Block diagram of the Realised Large Signal waveform Measurement and Engineering System

The triggering architecture, shown in figure 2 uses an Agilent Distribution box (Z5623A Option K08) originally provided by Agilent for coherently phase locking two sources together [6]. The signal sources procured for the measurement system have option HCC which routes the fundamental frequency of the internal YIG oscillator via the back panel. This path can then be broken and taken to the distribution Box where it is amplified and split providing two perfectly coherent outputs. One output is supplied back to the original source (the Master) and the other is intended for the other source (the Slave). However in the devised configuration the second output is routed to the trigger input of the DSA. Importantly the output of the YIG oscillator is always in a frequency range of 3.2 to 10 GHz, as the output occurs before the frequency doublers within the signal source. This means that the trigger frequency is always either at exactly the

same frequency or some sub-harmonic of the stimulus signal with perfect phase coherence and is always in the relevant frequency range of the trigger circuitry. This did however mean that the load-pull source and stimulus source had to be locked together using a standard 10 MHz reference signal (with the 44 GHz PSG as the fundamental source). However investigations indicated that this was all that was required as the drift between sources is not significant within a measurement period (tests showed that this method of locking the two sources limited the maximum number of averages to <512, due to relative frequency drift)

Measurement System Validation

To be useful a measurement system must have sufficient directivity (ability to distinguish between a high reflect and a match) and also be highly repeatable

between measurements. Figure 3 shows the raw performance when on-wafer match, open and short calibration standards are measured, the plot indicates impressive performance with at least 8 dB raw directivity over the 40 GHz bandwidth. Work is ongoing to reduce the loss between the reflectometer and the probe tips, which would further improve the raw directivity of the system, and thus improve overall system performance.

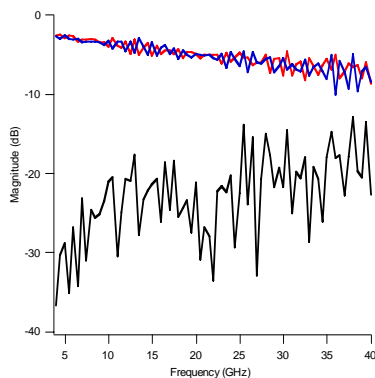


Figure 3 – Raw directivity of the realised measurement system

To show the repeatability of the measurement system, a one-port calibration was performed. The standards were then re-measured after calibration. The resulting magnitude of the s-parameters are shown in figure 4, good repeatability is observed with a noise floor of around 50 dB over the 40 GHz bandwidth.

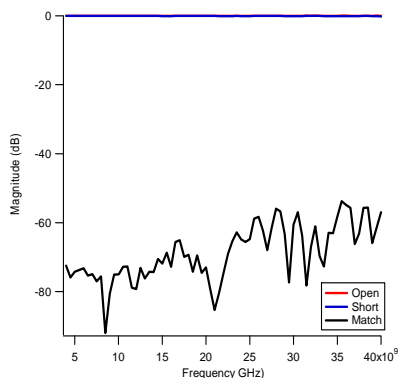


Figure 4 – Calibrated repeatability measurement

The final step in the validation process was to compare the magnitude and phase of measured input match of a passive antenna structure to those measured by a high quality Agilent 8510 Vector Network Analyser (VNA). The results are shown in figure 5 and highlight the excellent agreement in both magnitude and phase across the 40 GHz measurement bandwidth.

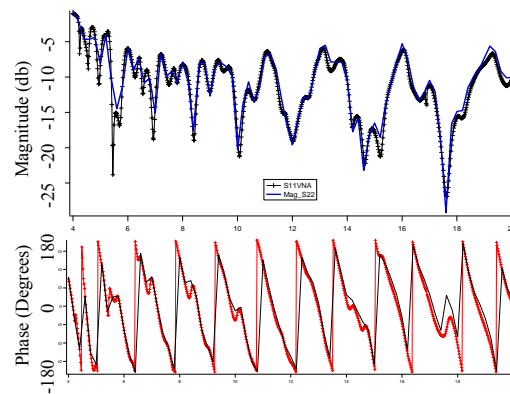


Figure 5 – Comparison between new measurement system and VNA

Device Characterisation

The measurement system described in the previous section was next used to fully characterise a 6 x 100µm GaAs transistor; the resulting measurement data is interesting from a number of perspectives, firstly it allows interrogation of the device performance, secondly it allows optimisation of matching circuit designs and finally as GaAs is a mature technology, the measurements can be used to validate the measurement system under large signal operation as we would expect the results observed to be in good agreement with theory.

The first measurement was performed to observe the dynamic RF load-line, achieved by plotting output voltage versus output current and to compare it to the DC boundary conditions, as the device is driven into compression. The result is shown in figure 6, and allows analysis of any dispersion caused by the device parasitics.

In this case little dispersion is observed, with virtually no difference between DC

and RF performance, this gives a good verification of large signal measurement system whilst providing positive feedback to the device manufacturer. This type of analysis becomes particularly useful when characterising new device technologies such as GaN transistors, where dispersion mechanisms become far more prevalent. It has been shown that using such analysis enables separation (removal) of the dispersion mechanisms allowing observation of both knee walkout and soft pinch-off [7-8].

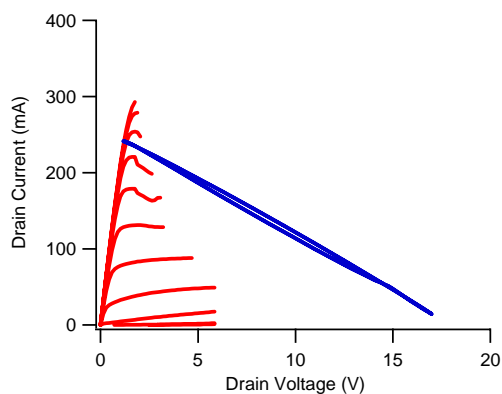


Figure 6 – Dynamic Load-line Analysis using measured RF and DC Performance

Importantly through extending the measurement frequency range these techniques can now be applied at much higher frequencies.

The measurement system can also be employed to perform automated power sweeps along with load-pull sweeps. Figure 7 shows the waveforms with the device biased in class B with 6 GHz stimuli, as a power sweep is conducted into a 50-Ohm impedance. The corresponding Pout versus Pin plot shown in figure 8. Further validation of the measurement system performance is achieved through observation of the waveform shape with the expected half rectified output current waveform confirming class B operation.

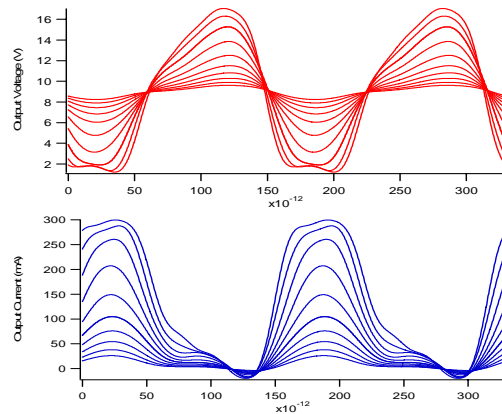


Figure 7 – Measured Class B Output Waveforms as the Device is driven into compression

By combining automated power sweeps with load-pull it is possible to create power dependent contour plots showing the gain, maximum output power and efficiency. For example Figure 9 shows the measured contours of Power Added Efficiency (PAE) 3dB into compression across a wide area of the Smith chart.

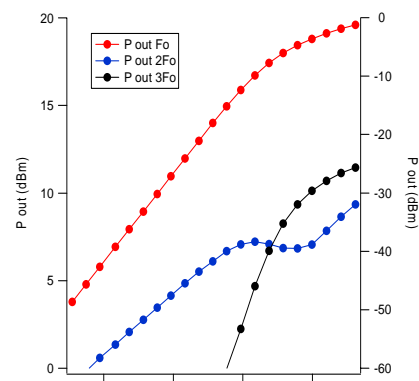


Figure 8 – Measured Power Performance into 50 Ohm

It should be noted that the contour plots shown in figure 9 give the device efficiency for impedance presented at the probe tips. The device is embedded between two line structures, it is therefore necessary to de-embed back to the device plane. Figure 10 shows the optimum device plane impedance required for maximum PAE at 5, 7.5 and 10 GHz after de-embedding.

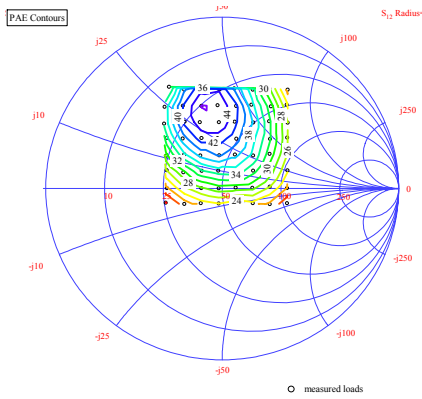


Figure 9 – Measured PAE Contours 1 dB into compression

Figure 10 again indicates very clean device performance with measurements agreeing excellently with theory for ideal device operation. It can be seen that the points lie almost perfectly on a circle of constant G of 0.55, and that the value of susceptance (B) doubles as expected with frequency. Such good agreement with theory also offers further validation of the large signal measurements.

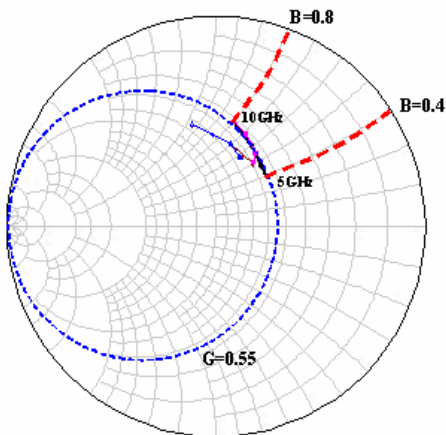


Figure 10 – De-embedded optimum impedance required for maximum PAE

This data can also clearly be used to design an optimum output matching circuit to maximise efficiency. Using the values of G and B at each frequency in a standard formulation shows that the matching circuit for optimum efficiency is required to resonate out an output capacitance of 0.3 pF and provide a real load of 91 ohms. The design and realisation of the matching

network will be covered in detail in the next section.

Matching Circuit Design

In this example the requirement was for a driver stage that can produce power in excess of 24dBm over the frequency range of 5-10 GHz. Maximising PAE is stated as being a key factor. To allow for comparison two different methods were employed while designing the required matching circuit. The first method employed a standard inter-stage circuit optimisation approach. The second method uses the more scientific approach and applies measured data directly in the design process. The device was characterised at 5, 7.5 and 10 GHz over an 8x8 impedance grid and over a 15 dB power range (up to 3dB of compression) and various load pull contours were plotted. Impedance values were chosen at each frequency to maximise PAE whilst still achieving the required output power, at 1dB compression. The results achieved are summarised in Table 1.

Frequency GHz	PAE %	Pout dBm	Load Mag/Ang
5	48.2	26.7	0.35/60.7°
7.5	47.1	26.5	0.40/79.9°
10	44.0	26.6	0.50/103.3°

Table 1. Loads chosen for best PAE and resulting Pout

These loads are the ideal values, and it may not be practical to realise these exact impedances within the design. Thus the next stage in the process is to import these values into a circuit simulator and determine what practical impedances can be achieved.

The resulting matching networks from the two approaches are shown in figure 11, it is clear that the design using the new measurement based approach (shown in pink) produces a response that is very different to a more standard design approach shown in red.

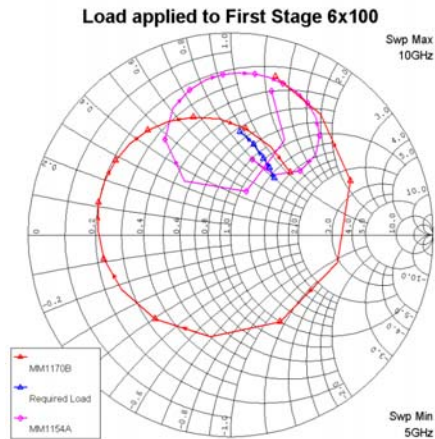


Figure 11 – Resulting matching circuit designed using the simple inter-stage matching and using the new measurement based approach

The two matching networks have now been emulated using the waveform measurement systems active load-pull capability and results suggest that the design using data from the new measurement system will give a more efficient circuit, although we are waiting for measurement of the actual circuits for final confirmation. Both designs are currently in production.

Conclusions

A new measurement system has been presented along with a full verification. The presented system allows various valuable design techniques developed over the past 10 years at lower frequencies, based around the commercial communication bands to be employed at higher frequencies in wider bandwidth military applications.

It has been shown that the data produced by the measurement system is useful in two areas; firstly it provides useful feedback to the device manufacturer where measurements can be used to uncover the cause of many problems; secondly by completing measurements under varying conditions it is possible to use the information directly in the design process, aided by a fully realised method for integration into a CAD environment. This allows for a more scientific and robust

design methodology that looks to supersede the standard MMIC design process. The new measurement based design process gives the designer significantly higher confidence in the performance of the circuit *prior* to committing to fabrication, significantly increasing the chance of a right-first-time design.

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