In-situ SiN passivation of X-band GaN power devices

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Abstract

GaN grown onto Si substrates offers a low cost, manufacturable route to the realisation of a power transistor technology with the potential to dramatically improve the performance of microwave power amplifiers. Although GaN HFET devices on Si have been demonstrated at QinetiQ with power densities of 2.8W/mm, they are still not able to match the performance of similar devices produced on SiC substrates. Here we report on experiments to study the effect of in-situ grown SiN on surface states, and thus current slump and knee-walk out effects which degrade GaN HFET device efficiency.

Keywords: GaN, AlGaN, Si, HFET, HEMT

Introduction

The ability of GaN to deliver FETs with superior break down voltages and therefore higher power devices has been successfully demonstrated in many laboratories [1-5]. In comparison to GaAs FETs, a GaN based technology is capable of providing at least five times more power, at frequencies up to 40GHz, as well as comparable RF noise performance with five times higher overdrive capability. Over the last few years, a number of devices based on this technology have become commercially available. However some significant challenges for the full productionisation of this technology still exist.

Due to the very high power capability of GaN, self-heating of devices is a significant issue and therefore the majority of GaN device development has taken place on SiC substrates which offer extremely good heat removal from devices. SiC is also a close lattice and thermal expansion coefficient match to GaN, which simplifies the epitaxial growth. However, SiC substrates are relatively expensive (about 100 times the cost of Si substrates) and are only recently becoming available in large diameters (up to 100mm) to allow current commercial device processing capabilities to be exploited.

The aim of this programme is to investigate the growth of GaN HFET structures onto Si substrates. This will offer an immediate, low cost route to commercialisation of this technology by delivering large diameter epitaxial wafers compatible with existing commercial device foundries. To date, the programme has focused on the demonstration of epitaxial structures and devices on 100mm Si substrates. Currently, preparations have started, including the purchase and installation of a new growth reactor at QinetiQ, to produce GaN based HFET structures onto 150mm Si substrates. This will provide layers suitable for processing trials of GaN FETs in existing UK foundry facilities.

In previous conference papers [6-9] we have demonstrated the growth of crack free epitaxial layers and the processing of devices giving up to 2.8Watts/mm. However, the output power and efficiency of these devices has been limited by an inability of the RF loadline to access the knee region of the device IV curves at high frequencies (known as "current-collapse"). This is shown in Figure 1 which shows a comparison between DC and load pull measurements on a GaN FET device on a Si substrate.

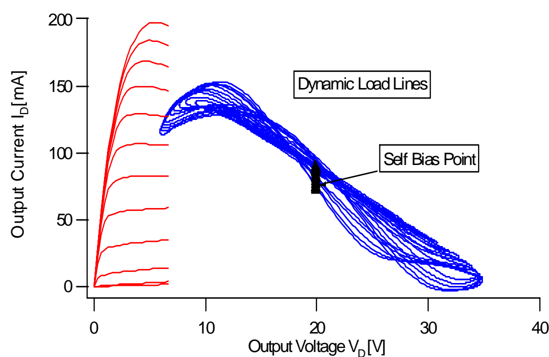

Figure 1. Fan diagram showing the 1.8GHz RF dynamic load lines (blue) and DC-IV curves (red) for 2x100µm devices operated under Class A conditions for a GaN on Si HFET. The power density of this device was 2.8 W/mm.

Device simulations [10] have suggested that the knee-walk out and current slump effects may be due to charge injection from the transistor gate into states on the AlGaN surface. From experience with devices on SiC, it is possible to partially overcome this effect using *ex-situ* SiN passivation. However, despite the fact that the device characterised in figure 1 has this passivation in place, it has not improved the device characteristic to the performance that would be observed for the same process applied to GaN FET's on SiC. The use of an *in-situ* nitride has the potential to change the situation as the AlGaN surface is encapsulated, *in-situ* in the growth reactor and therefore remove the possibility of oxidation or contamination of the epitaxial layer surface during processing.

To study the effects of *in-situ* passivation on device performance we have performed experiments to grow SiN onto HFET structures on sapphire substrates within the MOVPE growth reactor. The use of device layers on sapphire substrates was chosen, as the process of producing HFETs on sapphire is much more mature and would therefore allow the properties of the *in-situ* passivation to be better characterised and understood.

Growth of *in-situ* SiN passivation

The *in-situ* SiN used for passivation of the devices was deposited using SiH_4 and NH_3 immediately after the MOVPE growth of the standard HFET structure with a growth rate of about 0.05nm/sec. It can be seen from table 1 that the addition of the *in-situ* nitride has a negligible effect on the sheet resistivity of the layers, but the pinch off voltage measured using a mercury probe increases monotonically due to the increased distance from the layer surface to the 2DEG.

Wafer ID	**In-situ SiN thickness (nm)**	**Sheet resistivity (ohms/sq)**	**Vpinch (-V)**
A	0	512	5.1
B	2	515	5.9
C	25	499	15.4
D	50	481	29.3

Table 1: Electrical characteristics of HFET structures with varying thicknesses of in-situ SiN.

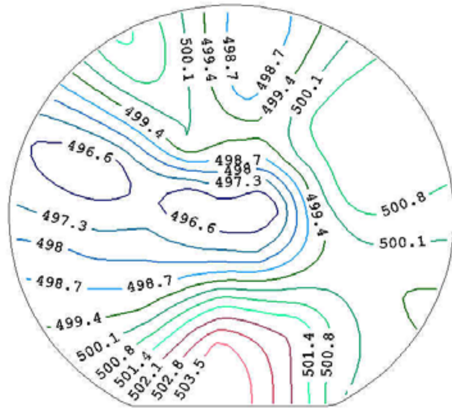

Figure 2: Sheet resistivity map of wafer C with 25nm of in-situ SiN. The uniformity of this wafer is better than 0.5%.

Figure 2 shows a resistivity map for wafer C which has 25nm of *in-situ* SiN and indicates good uniformity (<0.5%).

Device processing

Three types of device have been produced from the structures listed in Table 1. Firstly, a standard HFET structure which has no *in-situ* SiN (layer A) to provide a comparison for the *in-situ* passivated devices. Secondly, a MISFET structure which has 2nm of *in-situ* SiN under the gate (Layer B) and thirdly a device where the gate has been recessed through the 25nm thick *in-situ* SiN (Layer C). These devices were based on the standard device process developed at QinetiQ and described elsewhere [11]. For this third type of device, it was necessary to develop a low damage dry-etch process in order to allow the gate to be recessed through the SiN passivation. Several etch chemistries were investigated including CF_4/O_2, SF_6/Ar and CF_4/Ar. CF_4/Ar was found to be the most appropriate etch chemistry and gave a low etch rate allowing depth control, a good profile and a clean etched surface with no detrimental residues.

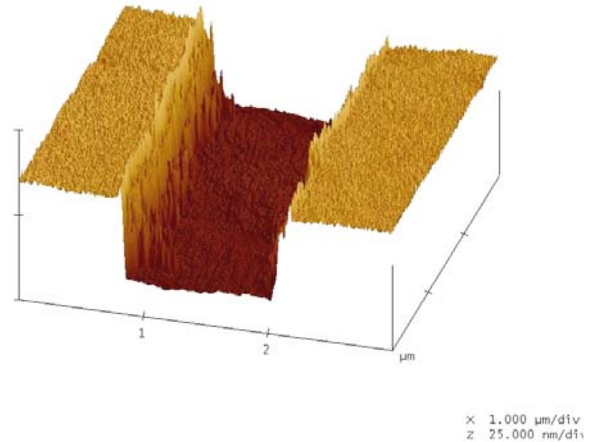

Figure 3: AFM image of the gate recess in the 25nm in-situ SiN. The measured recess depth is 24nm.

Figure 3 shows an AFM image of an etched recess in the *in-situ* SiN before gate deposition. The measured depth of the recess is 24nm in agreement with the measured thickness of the *in-situ* SiN and indicating that the etch has good selectivity between SiN and the AlGaN barrier layer.

Device results

Table 2 gives the DC results measured for the 3 types of device fabricated. Good DC device performance was obtained in all cases. It was found that the thin *in-situ* nitride significantly improve the gate leakage.

	Std HFET (no *in-situ* SiN)	**MISFET (2nm *in-situ* SiN)**	**Recessed FET (25nm *in-situ* SiN)**
Contact Rc (Ohm.mm)	0.17	0.36	0.16
Lg (µm)	1	1	1
I_{dss0} (mA/mm)	430	500	450
gm (mS/mm)	142	112	114
Vp (V)	-4.1	-5.4	-4.45
f_T (GHz)	9.5	9-11	9-12
Pre-passivation slump ratio (class B) (%)	Not tested	14	57
Post-passivation slump ratio (class B) (%)	87	81	93

Gate/drain reverse leakage @ -10V (mA)	0.15	up to 2e-6	up to 2e-3

Table 2: Small signal device parameters measured for devices with no in-situ SiN, 2nm in-situ SiN and 25nm in-situ SiN. All devices were subsequently passivated with ex-situ SiN.

Large Signal RF Measurements

Pulse IV and time domain RF loadpull measurements were used to assess the RF power performance of each process variant. The "slump ratio" given in Table 2 derived from the pulse IV data is a measure of current-collapse with 100% being ideal behaviour. It was found that the thin *in-situ* nitride was insufficient in itself to ensure good performance. A thick layer of passivation (either *in-situ* or *ex-situ*) was necessary to largely suppress the current-collapse.

The RF power density achieved at 1.8GHz was similar in all cases after passivation, with little improvement seen before and after applying the *ex-situ* nitride in the case of the recessed FET. Up to 3.2W/mm with a PAE of 48.8% was achieved in class B with V_{ds}=28V. Figure 4 shows the RF load-lines for the recessed device in class A conditions indicating that there is a small amount of dispersion for the fully passivated case.

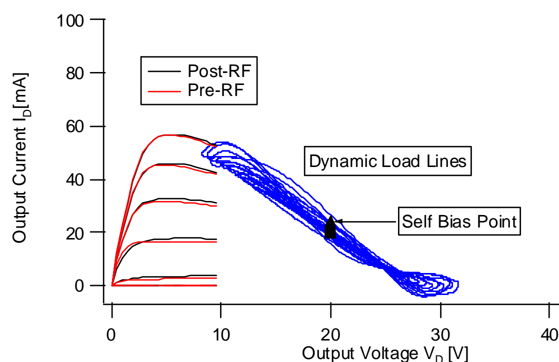

Figure 4: DC and RF load-lines for the recessed FET (2x50 μm) with both in-situ and ex-situ nitride measured at 1.8GHz under class A conditions.

Conclusion

In-situ nitride has been successfully and reproducibly deposited during the MOVPE growth of the epitaxial layer structure. This has been successfully incorporated into the QinetiQ GaN HFET process, including the demonstration of a low physical damage plasma etch process, with no obvious electrical damage or impact on process yield.

Although the nitride apparently improves the gate leakage, it seems that control of current-collapse and hence improved RF efficiency and output power requires more than just the control of the interface chemistry. Other factors remote from the surface interface need to be considered such as the in-built strain in the structure.

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