

## Recessed Gate GaN/AlGa<sub>N</sub> HFETs

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### Abstract

*In order to improve the high frequency performance of GaN/AlGa<sub>N</sub> HFETs the use of a GaN cap layer and gate recess device structure are investigated. Here we present the development of a selective etch recipe that is suitable for the fabrication of such devices. Two etch recipes, using Cl<sub>2</sub>/Ar/O<sub>2</sub> and SiCl<sub>4</sub>/SF<sub>6</sub> gas chemistries, have been investigated in terms of GaN and AlGa<sub>N</sub> etch rates and GaN:AlGa<sub>N</sub> selectivity. The SiCl<sub>4</sub>/SF<sub>6</sub> recipe has been identified as the most suitable for the fabrication of gate recessed HFETs, and GaN:AlGa<sub>N</sub> etch-rate selectivity of 14:1 has been achieved. The optimised etch recipe has been used in tandem with a three stage EBL process to fabricate gate recessed HFET devices, which have been characterised using DC and pulse measurements.*

Keywords: Gallium nitride, heterostructure field effect transistors, high frequency operation, recessed gate.

### Introduction

In recent years, there has been extensive interest in AlGa<sub>N</sub>/GaN HFETs for high power radio-frequency applications because of the wide bandgap, high breakdown field, high sheet carrier concentration and high saturation velocity. Devices with output power densities of 30W/mm at 8GHz on SiC substrates [1] and 12W/mm at 10GHz on Si substrates [2] demonstrate the realization of this potential.

Employing an n<sup>+</sup> GaN capping layer in the HFET structure can improve the source and drain ohmic contacts enabling reduced

parasitic access resistance which leads to improved performance under high frequency operation [3, 4]. However, the addition of the GaN cap can result in a reduction in the sheet charge in the 2DEG since the GaN cap will modify the spontaneous and piezoelectric polarisation charge distribution in the structure [5] and, because of the increased separation between the gate and channel, will decrease the transconductance. In order to minimise the effect of the first problem and overcome the second, a thin cap layer can be employed, which is then removed beneath the gate.

To achieve this, a dry etch recipe that is selective between GaN and AlGaN is required. As well as good selectivity, the recipe must also inflict minimal damage upon the underlying AlGaN layer, to ensure the integrity of the gate Schottky contact remains. The final requirement is a low etch rate, because the cap layer is necessarily thin. Several selective etch recipes have been reported in the literature to date. Etching of III-nitrides is typically performed using Cl<sub>2</sub> based gas chemistries and GaN:AlGaN selectivity has been achieved by introducing O<sub>2</sub> into the plasma [6-8]. The increase in selectivity is attributed to the formation of an Al-O layer on the AlGaN surface, which acts as an etch resistant barrier.

Here we report on the optimisation of a selective dry etch process, suitable for the fabrication of gate recessed HFETs. We have also fabricated recessed gate devices on 5nm n<sup>+</sup> GaN capped wafers using the optimised etch recipe.

#### **Experimental details**

The AlGaN/GaN layers were grown using metal-organic vapour phase epitaxy (MOVPE) on sapphire substrates. Etching experiments were carried out on 2.5µm thick GaN and Al<sub>0.25</sub>Ga<sub>0.75</sub>N layers. The HFET device structure consisted of a 1µm graded AlGaN buffer layer, followed by an undoped 0.5µm thick GaN buffer, an undoped 22nm thick Al<sub>0.25</sub>Ga<sub>0.75</sub>N barrier and a 5nm n<sup>+</sup> GaN cap.

The etching experiments were carried out using an Oxford Instruments Plasmalab ICP system, which incorporates a vacuum load lock to prevent atmospheric contaminants from affecting the etch. All etching was carried out on a 4 inch Si carrier wafer which was maintained at a constant table temperature of 20°C. An ICP power of 450W and RF powers between 10 and 150W were used. Etch depths were measured using a Dektak 3030

ST surface profiler with a resolution of ±5nm.

To fabricate the recessed gate HFETs the following procedure was used. The mesa device isolation (70-100nm depth) was achieved using ICP etching. Ti/Al/Ti/Au (20/100/45/55nm) ohmic contacts were thermally evaporated and annealed at 850°C for 30 seconds under N<sub>2</sub> ambient. Two further thermal evaporation steps were used to deposit Ni/Au (20/100nm) Schottky contacts and Ti/Au (20/200 nm) bond pads.

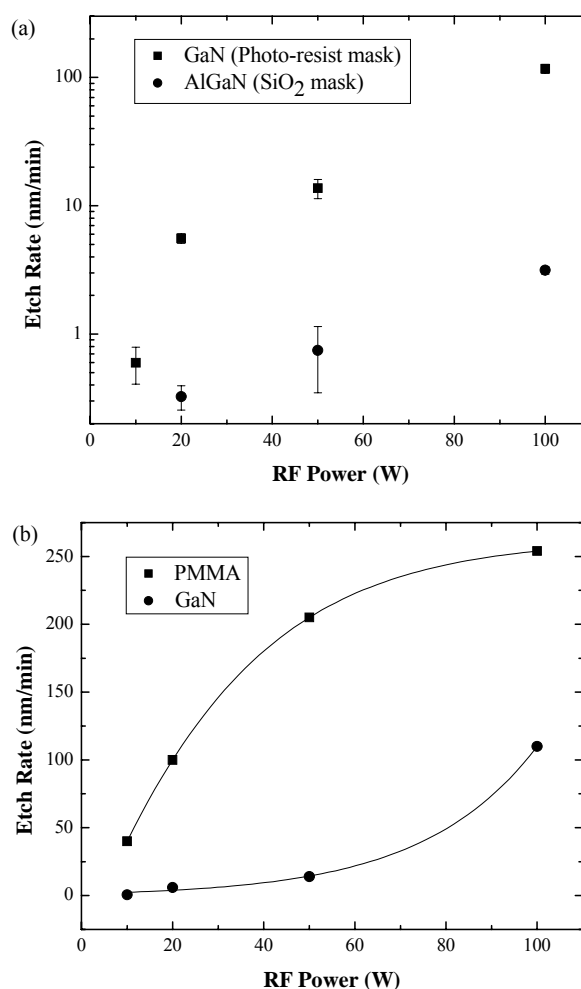
A three stage electron beam lithography (EBL) process was employed to fabricate the gate recess structure. In the first stage, two sets of alignment marks were defined using EBL and deposited using thermal evaporation. This enabled precise alignment of the gate to the recess in the subsequent processing steps. Secondly, the gate recess was defined and etched using the ICP system. Finally, the gate was defined at the centre of the recess and 20/100nm Ni/Au was evaporated. Devices were then passivated using 50nm SiN deposited using plasma enhanced chemical vapour deposition (PECVD).

#### **Results and Discussion**

Three etch recipes have been investigated with the emphasis on minimising etch rate and maximising GaN:AlGaN selectivity. Firstly, our conventional etch recipe, used during device fabrication for the mesa isolation step, was investigated. This recipe uses a mixture of Cl<sub>2</sub>/Ar/SiCl<sub>4</sub> with flow rates of 15, 4 and 1.5sccm respectively. The etch rates of GaN and AlGaN samples were investigated with a range of RF powers between 10 and 150W. At low powers the etch rate was suitably low, however the maximum selectivity achieved was just 1.3:1.

To improve selectivity, the conventional etch recipe was modified to include O<sub>2</sub>. A

gas mixture of  $\text{Cl}_2/\text{Ar}/\text{O}_2$  at flow rates of 30, 10 and 2sccm respectively was employed with a pressure of 10mTorr [7]. The ICP power was kept constant at 450W, whilst the RF power was varied from 10 to 100W. The GaN and AlGaIn etch rates are presented in figure 1(a). The GaN etch rates were readily obtained using a photo-resist mask, however, there was no observable etching of the AlGaIn, indicating a minimum selectivity  $>20:1$ . In order to obtain the true selectivity a 500nm thick  $\text{SiO}_2$  mask was used to allow longer etching times. Using the same conditions, but with longer etch times, it was possible to measure etch rates and the selectivity was found to be dramatically reduced to  $\sim 10:1$ . This drop in selectivity is attributed to sputtered Si from the  $\text{SiO}_2$  mask which getters  $\text{O}_2$  contained within the plasma and consequently results in a decrease in selectivity between samples. It is important to note that for  $\text{Cl}_2/\text{Ar}/\text{O}_2$ -based plasmas investigated in the literature a  $\text{SiO}_2$  mask is extensively used in order to enable an accurate figure for selectivity to be obtained. It is therefore proposed that, by using a resist mask, the quoted selectivity between GaN and AlGaIn could be dramatically improved.



**Figure 1.** GaN and AlGaIn etch rates (a) and GaN and PMMA etch rates (b) as a function of RF power for the  $\text{Cl}_2/\text{Ar}/\text{O}_2$  ICP etch recipe.

In order to fabricate gate recessed HFETs with sub-micron gate length, electron beam lithography must be used. Therefore, another important factor in developing a selective etch recipe, is that the etch rate of the PMMA resist mask is minimised. Figure 1(b) illustrates the PMMA etch rates as a function of RF power for the  $\text{Cl}_2/\text{Ar}/\text{O}_2$  recipe, with the GaN etch rates presented as a comparison. The selectivity of GaN:PMMA is found to increase with increasing RF power with the highest value of 0.43:1 at 100W. At these high RF powers the etch rate for both the GaN and PMMA are high, resulting in an impractically small etch time, making it

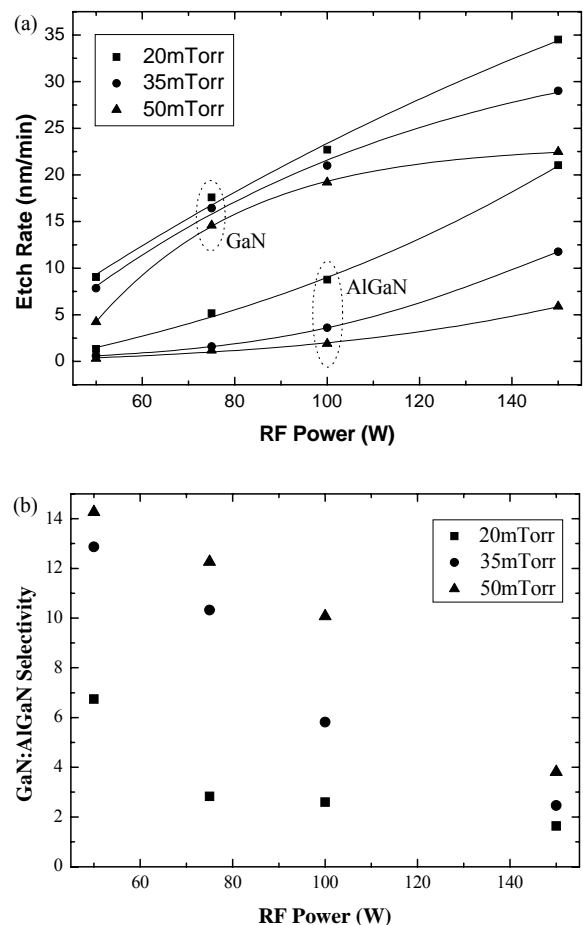
unsuitable for a gate recessed device. Therefore, the use of lower RF powers where the etch rate for the GaN is reduced giving a more controllable rate is advantageous. However, under these conditions the GaN:PMMA selectivity is 0.015:1, which is not suitable for the gate recess etching.

For this reason, a third etch recipe was investigated. Recipes using a mixture of  $\text{SiCl}_4/\text{SF}_6$  have been used extensively in AlGaAs/GaAs material systems [9]. By incorporating  $\text{SF}_6$  into the plasma recipe the obtained selectivity between GaAs and AlGaAs is achieved through the reaction of fluorine with aluminium contained within the AlGaAs material which forms a layer of  $\text{AlF}_3$  on the surface and acts as an etch resistant barrier. Figure 2 shows the etch rates and selectivity for bulk GaN and AlGaN samples etched using the  $\text{SiCl}_4/\text{SF}_6$  recipe. The flow rates were 20 and 5sccm for  $\text{SiCl}_4$  and  $\text{SF}_6$ , respectively. The ICP power was kept constant at 450W, whilst the RF power and chamber pressure was varied.

The etch rates of both GaN and AlGaN decrease with decreasing RF power and with increasing pressure. The maximum selectivity of 14:1 was achieved using a chamber pressure of 50mTorr and an RF power of 50W. Using these conditions the etch rate of the GaN is  $\sim 4\text{nm/min}$ , which makes it suitable for the gate recessing process. The reduction in selectivity for increasing RF power is attributed to enhanced sputtering of the induced Al-F film at the surface of the AlGaN layer. Under these high RF power conditions it is believed the etch mechanism is dominated by physical ion bombardment. As the RF power is reduced the selectivity improves, indicating a transition to a more chemical etching mechanism.

From figure 2(b) it can be seen that in addition to reducing the RF power, the

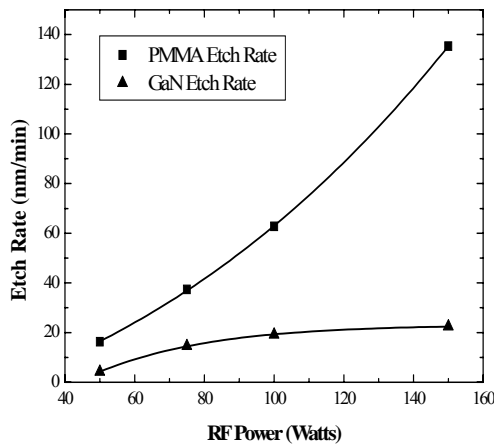
selectivity can also be controlled by altering the pressure in the ICP chamber. As the pressure is increased the mean free path of incident ions in the plasma is reduced and as a result their mobility is also decreased. Therefore, incident ions impinging on the AlGaN surface have less energy, preventing the removal of the etch resistant barrier layer. Consequently, etching under high pressure conditions and at reduced RF powers leads to increased selectivity between GaN and AlGaN films.



**Figure 2.** GaN and AlGaN etch rates (a) and GaN:AlGaN selectivity (b) as a function of RF power for the  $\text{SiCl}_4/\text{SF}_6$  ICP etch recipe.

As with the  $\text{Cl}_2/\text{Ar}/\text{O}_2$  recipe, the etch rate of PMMA in the  $\text{SiCl}_4/\text{SF}_6$  recipe was also assessed. Figure 3 shows the PMMA etch rate as a function of RF power when etching with a chamber pressure of 50mTorr. Using an RF power of 50W, the

GaN:PMMA selectivity is 0.26:1, which represents an order of magnitude improvement over the low power  $\text{Cl}_2/\text{Ar}/\text{O}_2$  recipe and is suitable for etching the gate recess structure.

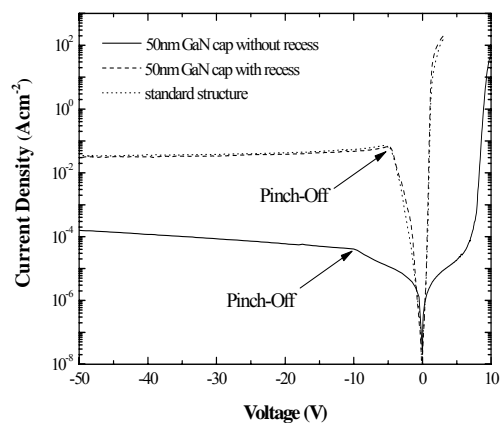


**Figure 3.** GaN and PMMA etch rates as a function of RF power for the  $\text{SiCl}_4/\text{SF}_6$  ICP etch recipe.

In order to quantify the damage induced from the optimised etch recipe and also confirm the selectivity between the GaN and AlGaN films, Schottky diodes were fabricated using HFET material with a 50nm undoped GaN cap. A recess was etched beneath the Schottky contact using the optimised  $\text{SiCl}_4/\text{SF}_6$  etch recipe for a period of 60 minutes, resulting in a 600% over-etch time. The diode performance is presented in figure 4, along with the characteristics for Schottky diodes fabricated without a recess and on standard AlGaN/GaN HFET material.

Schottky diodes formed on the 50nm GaN capped HFET material without recessing exhibited extremely low leakage currents when compared to conventional devices. This is because the effective barrier height is increased due to the modification of the piezoelectric and spontaneous polarisation in the structure resulting from the thick GaN cap [5]. This is confirmed by a greatly reduced current in the forward direction at a given voltage compared to material without the cap. Furthermore, the

diodes without a recess have a relatively high pinch-off voltage of  $\sim 10\text{V}$ , which can be attributed to the increased separation between the Schottky contact and the channel. By removing the GaN cap beneath the Schottky contact, using the optimised etch recipe, the pinch-off voltage was reduced to  $\sim 6\text{V}$ , which is consistent with the reduced Schottky-channel separation and coincides with the pinch-off for the standard HFET structure.



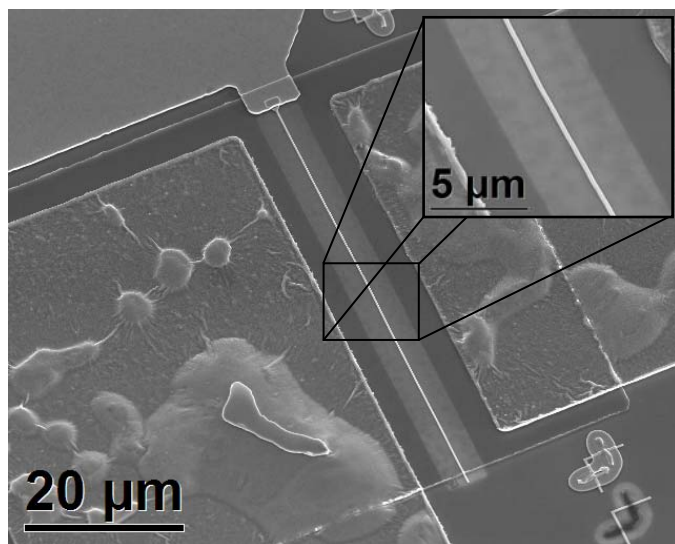
**Figure 4.** I-V characteristics for a recessed GaN/AlGaN/GaN Schottky diode compared to a conventional AlGaN/GaN rectifier.

The I-V characteristics for recessed and standard devices were almost coincident, which shows the etch was successful in removing the GaN cap, whilst introducing minimal damage into the device. It is believed the formation of the  $\text{AlF}_3$  layer on the AlGaN surface acted not only as an etch resistant barrier but also formed a protective covering on the surface of the semiconductor which prevented ion induced damage once the barrier layer was exposed.

The optimised  $\text{SiCl}_4/\text{SF}_6$  recipe has been utilised in the fabrication of gate recessed HFETs on GaN capped material. Figure 5 shows an SEM image of a gate-recessed HFET device with a 250 nm gate length. This device incorporates a 5  $\mu\text{m}$  long recess, which is far longer than necessary but facilitates easy observation and verifies

that the recess etch was successful. However, devices were also fabricated with recess lengths in the range of 0.3-1  $\mu\text{m}$ .

The sheet resistance and contact resistances were determined from TLM measurements to be  $576 \Omega/\square$  and  $0.38 \Omega\text{mm}$  respectively. This compares to sheet resistance of  $500 \Omega/\square$  and contact resistance of  $0.72 \Omega\text{mm}$  for standard HFET material processed at the same time. The significant improvement in contact resistance demonstrates the importance of the GaN cap layer in reducing parasitic access resistance.

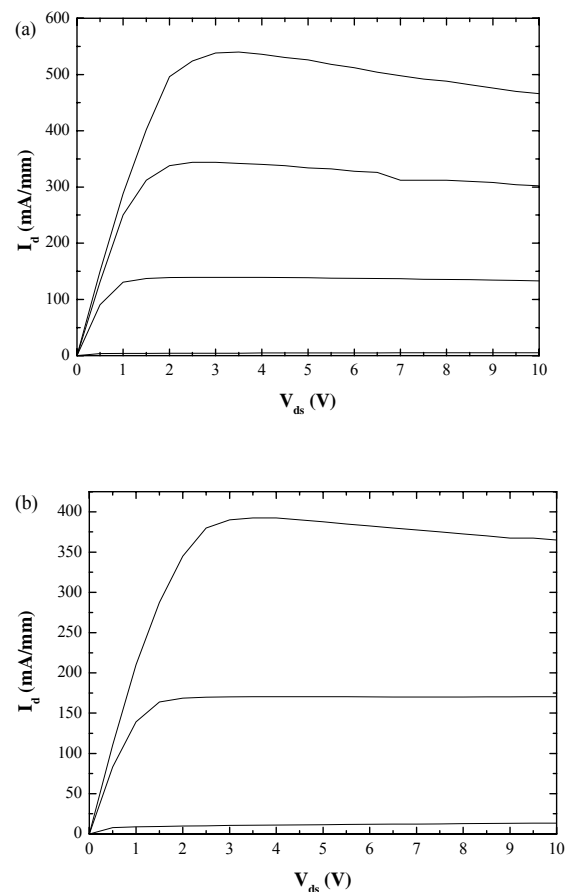


**Figure 5.** SEM Image of a gate recessed HFET.

The increase in sheet resistance can be explained by a reduction in the 2DEG sheet carrier concentration because of a modification of the spontaneous and piezoelectric polarisation charge distribution in the structure. For GaN/AlGaN/GaN structures a negative piezoelectric polarisation charge will be induced at the upper GaN/AlGaN heterointerface which will increase the electric field across the AlGaN and reduce the number of electrons in the 2DEG. However, this reduction in carrier concentration results in an increase in mobility from  $1050 \text{ cm}^2/\text{Vs}$  in the standard

structure to  $1360 \text{ cm}^2/\text{Vs}$  in the GaN capped material.

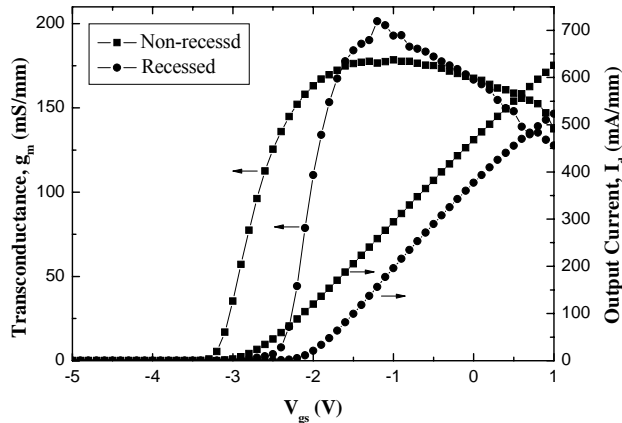
FET characteristics for a recessed gate device and a device with the gate deposited directly on top of the GaN cap (non-recessed) are shown in figure 6. The non-recessed device has a maximum output current of  $540 \text{ mA/mm}$ , which decreases to  $400 \text{ mA/mm}$  for the gate recessed device. The origin of this decrease in output current is unclear, however, it could be due to damage inflicted beneath the gate by the recess etch.



**Figure 6.** FET characteristics of (a) non-recessed and (b) gate recessed devices.

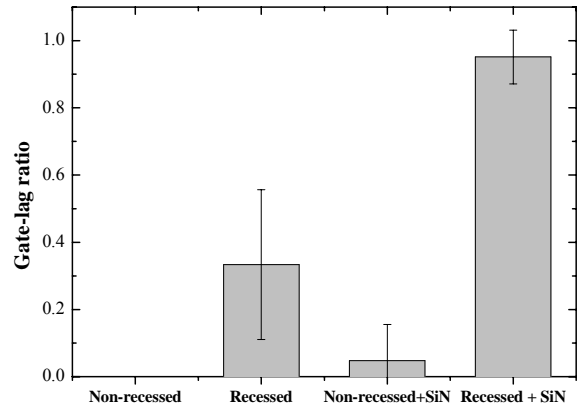
The transconductance and transfer characteristics for the recessed and non-recessed devices are shown in figure 7. A clear decrease in pinch-off voltage is observed for the recessed device, which

can be attributed to the decrease in gate-channel separation. The decrease is  $\sim 21\%$ , which is consistent with the 19% change in separation resulting from removing the 5nm cap layer. There is also an increase in maximum transconductance from  $\sim 180\text{mS/mm}$  to  $\sim 200\text{mS/mm}$ .



**Figure 7.** Transconductance and transfer characteristics for non-recessed and recessed HFETs.

The devices were also assessed using pulse measurements, which were performed at constant  $V_{DS}$  potential of 6V.  $V_{GS}$  is then kept at or below pinch off and the gate is pulsed to the full channel current. For these experiments the pulse length used was 400ns with a low repetition rate in order to minimise self heating. The output drain current is then normalised to the DC value giving the gate lag ratio (GLR). A GLR of one represents the ideal response and a ratio of zero indicates complete current collapse in the structure. The recessed and non-recessed devices were measured before and after SiN passivation and the results are summarised in figure 8.



**Figure 8.** Histogram showing gate-lag ratio measurements for non-recessed and recessed HFETs before and after SiN passivation.

Before passivation, the current collapse is very severe, with complete current collapse observed in the non-recessed devices and a gate-lag ratio of  $\sim 0.3$  for the recessed devices. After passivation, the non-recessed devices show only a marginal improvement, however, the recessed devices show almost no shortfall in output current.

### Conclusions

We have demonstrated two selective etch recipes suitable for the fabrication of gate recessed GaN/AlGaIn/GaN HFETs. The  $\text{SiCl}_4/\text{SF}_6$  recipe was identified as the most suitable in the fabrication of gate recessed HFETs due to the lower etch rate of PMMA and was shown to inflict minimal damage on the underlying semiconductor. The optimised etch recipe uses an RF power of 50W and chamber pressure of 50mTorr, resulting in a GaN:AlGaIn etch selectivity of 14:1. The optimised etch recipe has been used in tandem with a three stage EBL process to fabricate gate-recessed HFET devices. These devices demonstrated significant improvements in contact resistivity compared to uncapped structures and showed a gate lag ratio close to unity after passivation.

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