

Understanding Surface and Bulk Leakage Mechanisms in AlGa_xN/GaN HFETs

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Abstract

A surface leakage test structure is used to isolate the surface and bulk leakage currents in AlGa_xN/GaN based devices. Passivation of post-processed devices with stoichiometric Si₃N₄ resulted in reduced surface leakage, which suggests that surface passivation acts to suppress the AlGa_xN surface conduction, possibly through a reduction in surface states. However, passivation with low temperature grown SiN_x, which has a high density of interfacial states increased the surface leakage component instead. This implies that surface conduction is critically dependent on the amount of surface states present. The surface leakage component is also found to be thermally activated with an activation energy of 0.19 eV. When the devices are driven to hard breakdown, a sharp rise in the surface current is typically observed, which strongly suggests that breakdown in these devices is dominated by surface edge effects.

Keywords: AlGa_xN/GaN HFETs, SiN_x Passivation, Surface Leakage, Bulk Leakage

Introduction

Al_xGa_{1-x}N/GaN heterostructure field-effect transistors (HFETs) have been extensively exploited over recent years, due to their potential for high power, high voltage and high temperature applications. The presence of strong spontaneous and piezoelectric polarization charges in this material system yields high sheet densities of $n_s \sim 1 \times 10^{13} \text{ cm}^{-2}$ ($x=0.3$), without intentional doping. The breakdown field of GaN is estimated to be $\sim 3 \text{ MV cm}^{-1}$, which is ten times larger than that of GaAs. GaN also displays high electron saturation velocities ($v_{sat} = 2 \times 10^7 \text{ cms}^{-1}$). These desirable properties have resulted in very impressive output power densities of 16.5

W/mm at 10 GHz (on SiC) being achieved¹.

Despite this rapid development, little has been reported on the behaviour of the gate leakage current in these devices. Upon surface passivation, a sharp rise in gate leakage current is typically observed²⁻³, which may have consequences for noise sensitive applications. However, the origin of this detrimental effect is still unknown and little has been done to identify the root of this problem. In a conventional HFET, the gate leakage current should consist of a surface, bulk and mesa edge leakage component but efforts to differentiate these components are still lacking. In this paper, we present a novel surface leakage test structure used to isolate the surface and bulk leakage components. The devices

were subsequently characterised at elevated temperatures and passivated with SiN_x to provide further insight into the leakage and breakdown mechanisms under these conditions.

Growth and Device Fabrication

The device structure consists of a 30 nm thick AlGa_{0.25}Ga_{0.75}N and a 1.2 μm thick GaN buffer grown on a sapphire substrate. The HFETs were fabricated using a conventional route of mesa isolation, ohmic metallisation, gate metallisation and bond pad metallisation (Fig. 1). The isolation mesa was etched using inductively coupled plasma (ICP) to a depth of ~ 200 nm and the ohmic contacts consist of Ti/Al/Ti/Au, annealed at 850°C for 20 seconds. The gate contacts are formed using Ni/Au and Ti/Au used for bond pads. SiN_x dielectric films (~ 50 nm thick) were then deposited on post-processed HFETs in a commercial plasma enhanced chemical vapour deposition (PECVD) system. High temperature measurements were conducted in a furnace under flowing N_2 ambient.

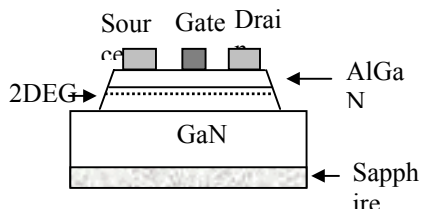


Fig. 1. Schematic device structure of AlGa_{0.25}Ga_{0.75}N/GaN HFET.

Surface Leakage Test Structure

The test structure (Fig. 2) consists of two Schottky contacts (gate and guard) and an ohmic contact. The gate is reverse biased in normal operation (typically swept from 0V to -100V) and the current that flows into the guard contact monitored. Since the guard is kept at 0V, the same potential as the 2DEG, any current that flows into it

must be a surface component. If the resistances of R3 and R5 are comparable, the apparent surface leakage component (I_{surf}) will be proportional to the gate leakage current (I_g) and the ratio of I_{surf}/I_g will be a constant.

Under these conditions, surface leakage will not be detected. However, under most circumstances, R3 has a high resistance at zero bias (note that the AlGa_{0.25}Ga_{0.75}N barrier directly beneath the Schottky guard contact will be fully depleted), thus I_{surf} will not be proportional to I_g . In this scenario, the I_{surf} current represents a real surface leakage component.

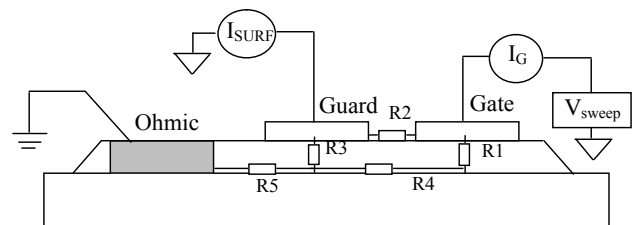


Fig. 2. Surface test leakage structure used to isolate the surface and bulk leakage components. The surface leakage component is monitored through the guard contact.

For this work, an inter-digited structure was used (Fig. 3) to maximise the surface periphery, and the gate contacts placed on-mesa and with no mesa edge crossings to eliminate the mesa edge leakage component. Hence, the gate current will consist of both the surface and bulk leakage components, while the guard current is the surface leakage component alone.

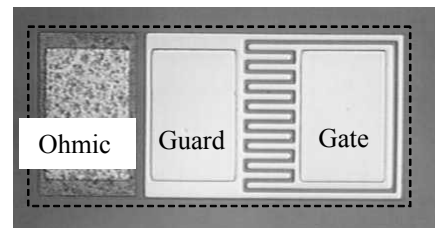


Fig.3. Surface test leakage structure. The mesa edge is represented by the dotted lines. The guard contact encloses the gate to ensure that there is no possibility of a surface leakage route from the gate to the ohmic contacts.

Results and Discussion

The surface leakage component is found to be dependent on the device configuration, and is also sensitive to the surface conditions. Note that special surface treatments were not employed on these devices. Higher surface leakage currents are typically observed on structures with large periphery to area ratios, such as, for example, on inter-digitated gates compared to annular Schottky diodes. For the inter-digitated structures, a rapid increase in I_{surf} is observed with increasing reverse bias but the bulk leakage current is clearly the dominant component at lower voltages (dark curves in Fig. 4).

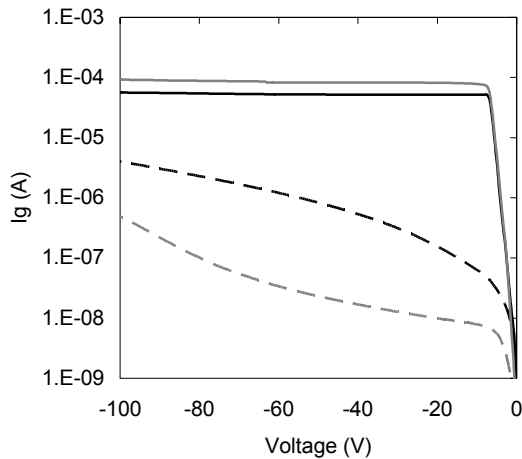


Fig. 4. Plot of I_g (solid) and I_{surf} (dashed) before (dark) and after (light) stoichiometric Si_3N_4 passivation.

The inter-digitated test structures were then used to provide further insight into the leakage mechanisms upon passivation with three different SiN_x variants. Fig. 4 shows the results obtained for devices before and after passivation with stoichiometric Si_3N_4 (Std-SiN). From the graph, the total gate leakage current increases upon passivation, but a striking feature observed is the I_{surf} variation. I_{surf} reduces by approximately 1-2 orders of magnitude when passivated with Std-SiN.

Before we proceed further, it is important

to emphasise that AlGaIn/GaN based HFETs suffers from ‘current collapse’, which translates into reduced output power at RF compared to DC⁴. The phenomenon is widely believed to be due to trapping effects along the ungated AlGaIn surface. However, surface passivation with SiN_x is shown to be able to mitigate these effects⁵ through a reduction in the density of surface states. A good technique used to detect the presence of ‘surface-related traps’ is through gate pulse measurements⁵ (imitates RF performance) and Fig. 5 shows the effectiveness of three different SiN_x variants in suppressing these effects on $1\mu\text{m}$ gate length HFET devices.

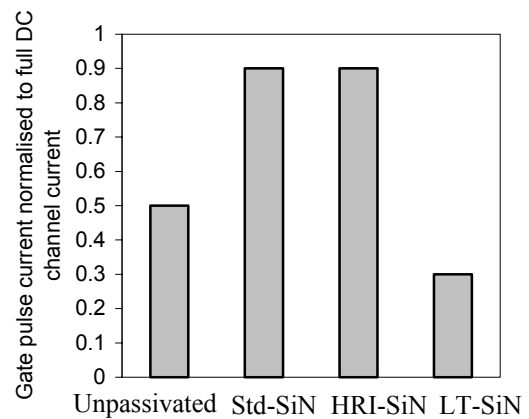


Fig. 5. Plot of gate pulse current normalised to the DC full channel current. The pulse width used is 400 ns at a frequency of 100 Hz, and the device is held at pinch-off ($V_{gs} = -5\text{V}$) when no pulse applied.

From Fig. 5, it is evident that both Std-SiN and high refractive index SiN (HRI-SiN) are very effective in mitigating electron trapping, but the low temperature deposited SiN (LT-SiN) is very poor in doing so, making the effect worse instead. The results from Fig. 4 and Fig. 5 would suggest that the Std-SiN film ‘passivates’ the electrical states along the ungated AlGaIn surface, which subsequently reduces surface conduction. Nevertheless, a net increase in the total leakage current is observed after passivation. This indicates that the rise in leakage current after passivation is a consequence of increased

bulk leakage contribution (I_{bulk}) and not surface conduction.

Next, the devices are passivated with LT-SiN. The LT-SiN is grown at 40°C instead of the conventional 300°C. Reducing the substrate deposition temperature acts to increase the density of interfacial states (D_{it}) and the consequence is the degradation in high frequency device performance. Therefore, devices passivated with LT-SiN resulted in more severe current collapse compared to when unpassivated and this is evident in Fig. 5. Using the Terman method ⁶, D_{it} values up to $5 \times 10^{12} \text{ cm}^{-2}$ and $\sim 10^{11} \text{ cm}^{-2}$ were measured on LT-SiN and Std-SiN metal-insulator-semiconductor (MIS) diodes respectively. This magnitude of D_{it} is significant on the former and confirms the presence of a large number of surface states on LT-SiN devices. However, the low D_{it} values on the latter suggest that a high quality interface exists on the Std-SiN/AlGaIn interface.

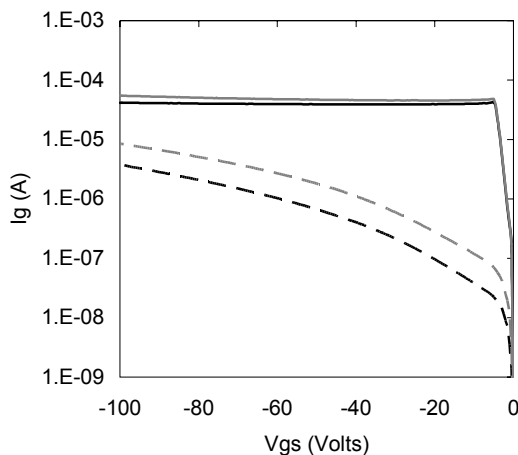


Fig. 6. Plot of I_g (solid) and I_{surf} (dashed) before (dark) and after (light) low temperature deposited SiN_x passivation.

Fig. 6 shows the results obtained when the devices are passivated with LT-SiN. It can clearly be observed that, contrary to the case of Std-SiN, I_{surf} increases instead after LT-SiN passivation. This strongly suggests

that surface leakage conduction is heavily dependent on the amount of states on the AlGaIn surface. Reducing the amount of surface states through passivation with the high quality Std-SiN films resulted in reduced surface conduction and vice versa for the poor quality LT-SiN. The rise in total gate leakage current is minimal compared to Std-SiN and this is attributed to the moderation of peak gate electric field resulting from the excess surface states created by LT-SiN ⁷.

An addition to this study is the use of high refractive index SiN_x film (HRI). This SiN_x variant is found to be excellent in improving breakdown voltage and better Class B operation compared to Std-SiN and is grown by reducing the NH_3 flow rate, thus leading to a Si-rich film. The results are shown in Fig. 7 and similar to Std-SiN, with an overall net increase in total leakage current is observed upon passivation. However, I_{surf} remains almost unchanged at low gate biases but increases at high biases. Since results from gate pulse measurements indicate that HRI-SiN is very effective in mitigating current slump, this would imply that surface states are also reduced in this case. We believe that the higher I_{surf} is not due to conduction along the surface states in this case, but due to enhanced hopping conduction within the Si-rich films instead and this conduction is enhanced at higher gate biases.

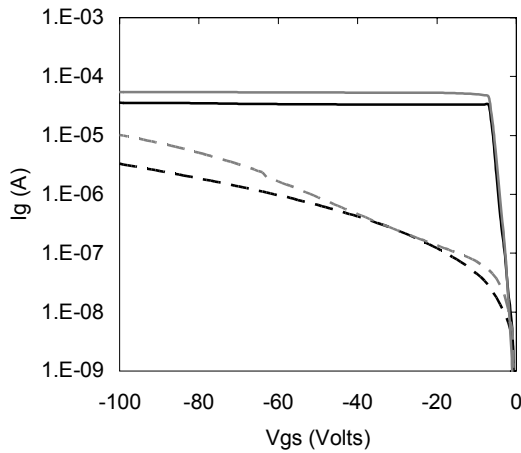
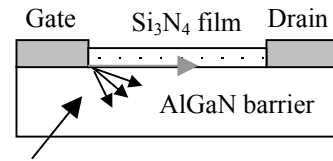


Fig. 7. Plot of I_g (solid) and I_{surf} (dashed) before (dark) and after (light) HRI SiN_x passivation.

To understand the origin of the bulk leakage rise upon passivation, surface test leakage structures comprising annular Schottky diodes with varying diameters are used. Beyond pinch-off, a linear dependence is obtained between I_{bulk} and diode periphery⁷, which indicates that the major I_{bulk} contributor is due to edge effects and not the area term. This observation leads us to believe that the rise in I_{bulk} after SiN_x passivation is a direct result of increased leakage injection at the gate edge.

Indeed, it is difficult to associate SiN_x passivation with increased leakage injection from ‘area’ bulk effects, since the area of the diode is essentially shielded by the gate metal and is not expected to be affected by the dielectric. When the devices are encapsulated, the leakage path along the surface is essentially cut-off due to ‘passivation’ of the surface states, hence leakage electrons are injected through the ‘edge’ bulk route instead. Fig. 8 illustrates a schematic diagram of the proposed leakage mechanism upon Si_3N_4 passivation.



Increased edge injection upon SiN_x passivation. Since surface conduction is reduced, leakage current conducts through the bulk instead.

Fig. 8. Schematic diagram of leakage mechanism when passivated with stoichiometric Si_3N_4 .

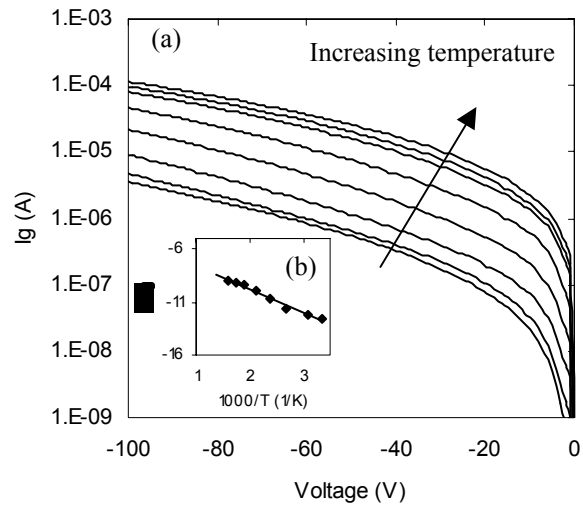


Fig. 9. I - V behaviour of (a) I_{surf} component as a function of temperature (20°C , 50°C , 100°C , 150°C ... 350°C). (b) activation energy plots at $V_g = -100\text{V}$.

Fig. 9 shows the surface leakage current for the unpassivated devices plotted as a function of temperature from 20°C up to 350°C . A rapid rise in I_{surf} is observed with increasing temperature and I_{surf} is also found to be thermally activated with an activation energy of ~ 0.19 eV (beyond pinch-off). This is a typical characteristic of hopping conduction taking place along the AlGaIn surface and is in good agreement with our previous interpretation⁸.

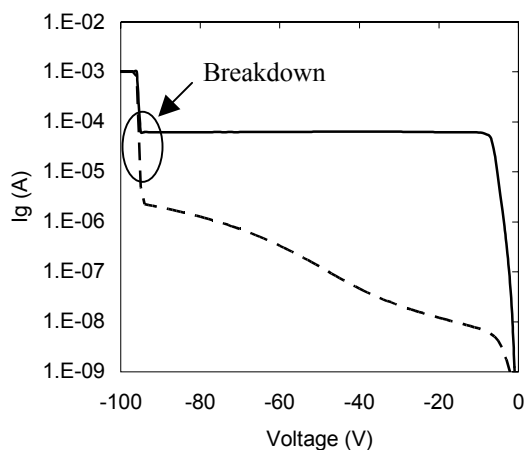


Fig. 10. The behaviour of I_g (solid) and I_{surf} (dotted) of a Si_3N_4 passivated device when driven to hard breakdown.

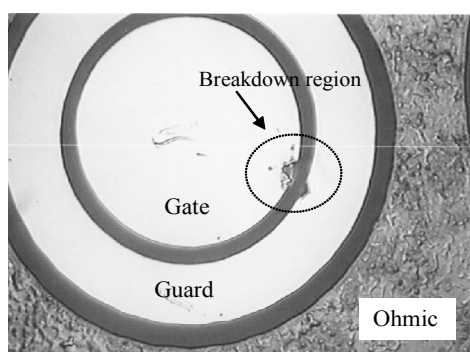


Fig. 11. Optical microscope image of a Schottky diode surface leakage test structure when driven to hard breakdown.

When the devices are slowly driven to hard breakdown (room temperature), a surge in I_{surf} typically occurs just prior to breakdown (Fig. 10). This behaviour occurs in both unpassivated and Si_3N_4 passivated devices, which strongly suggests that breakdown in these devices is dominated by surface edge effects. Fig. 11 shows an optical microscope image of edge breakdown on annular Schottky diodes. Note the damage on the guard as well as the gate when edge breakdown occurs.

Summary and Future Directions

The novel surface leakage test structure

has provided insight into the leakage mechanisms of AlGaIn/GaN heterostructures at high temperatures and upon SiN_x passivation. The surface leakage current is found to be dependent on electrical states present on the bare AlGaIn surface. Passivation with stoichiometric Si_3N_4 and LT-SiN showed a good correlation between the effectiveness of passivation in mitigating current collapse and the amount of surface conduction due to surface states taking place. The net increase in total leakage current when passivated is a result of increased edge leakage injection at the gate periphery. I_{surf} is found to be higher in HRI-SiN compared to Std-SiN, but its effectiveness in mitigating current collapse would suggest that hopping conduction could be taking place within the Si-rich dielectric films.

High temperature measurements also revealed that I_{surf} is thermally activated with an activation energy of ~ 0.19 eV. A sudden surge in I_{surf} prior to hard breakdown would indicate that surface related edge effects may be responsible.

Although we have demonstrated that surface conduction requires surface states, the relation between breakdown voltage and the magnitude of I_{surf} is still unclear. Further experiments are necessary in order to verify this. The use of different surface cleaning conditions in influencing I_{surf} would also be of interest. An RF-capable surface leakage test structure would enable studies of how surface and bulk leakage currents directly affect the HFET high frequency performance.

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