

Temperature Dependence of CPW Multilayer Inductors and capacitors

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Abstract

The growing popularity for multilayer CPW based components in MMICs requires a detailed characterization of these devices. We present here an experimental characterization of CPW multilayer inductors and capacitors over a wide range of temperature (-25 to 200°C) and frequency (45 MHz to 40 GHz). All structures are fabricated on GaAs semi-insulating substrate. The results show that the capacitance and inductance values remain unchanged, where as the Q factor of the inductor decreases by 25 to 40% over the temperature range due to the resistive losses. However the resonant frequency of the inductors remains constant with increase in temperature.

Keywords: CPW Multilayer, MMIC, Spiral inductor, Capacitor

Introduction

The CPW based multilayer technology is becoming a key factor in reducing the chip area and fabrication cost of MMICs. This is because the formation of thin-film multilayer structures on substrates offers high packaging densities and layout flexibility. Components such as inductors and capacitors are commonly used with active devices for impedance matching, phase shifting and biasing. Placed close to the active devices, these matching devices occupy most of the chip area increasing the cost of the chip. While the multilayer technology components can be placed on different layers reducing the area and thus increasing the density allowing multi module systems to be developed on the same wafer. However a comprehensive study of thermal characteristics of these components is required in order to assess their thermal properties.

Figure 1 shows the cross-sectional and micrograph of the fabricated multilayer CPW based inductors and capacitors. In this

work planar, offset stacked and directly overlaid inductors and multilayer capacitors of different areas are characterized over temperature and frequency.

The structures are fabricated on GaAs semi-insulating substrates with gold as the conducting layer and polyimide as the insulating layer. Metal thickness of $0.8\ \mu\text{m}$ and a polyimide thickness of $2.5\ \mu\text{m}$ are used in development of the 3-D MMIC components. On-wafer RF measurements are carried out using HP8510C Network Analyser.

Design and analysis

Multilayer Capacitors

Both overlay (metal-insulator-metal) and interdigitated capacitors can be used in MMICs [1]. Interdigitated capacitors are used for values up to 1 pF, above which the size and parasitics of the capacitor limits its application in MMIC circuits.

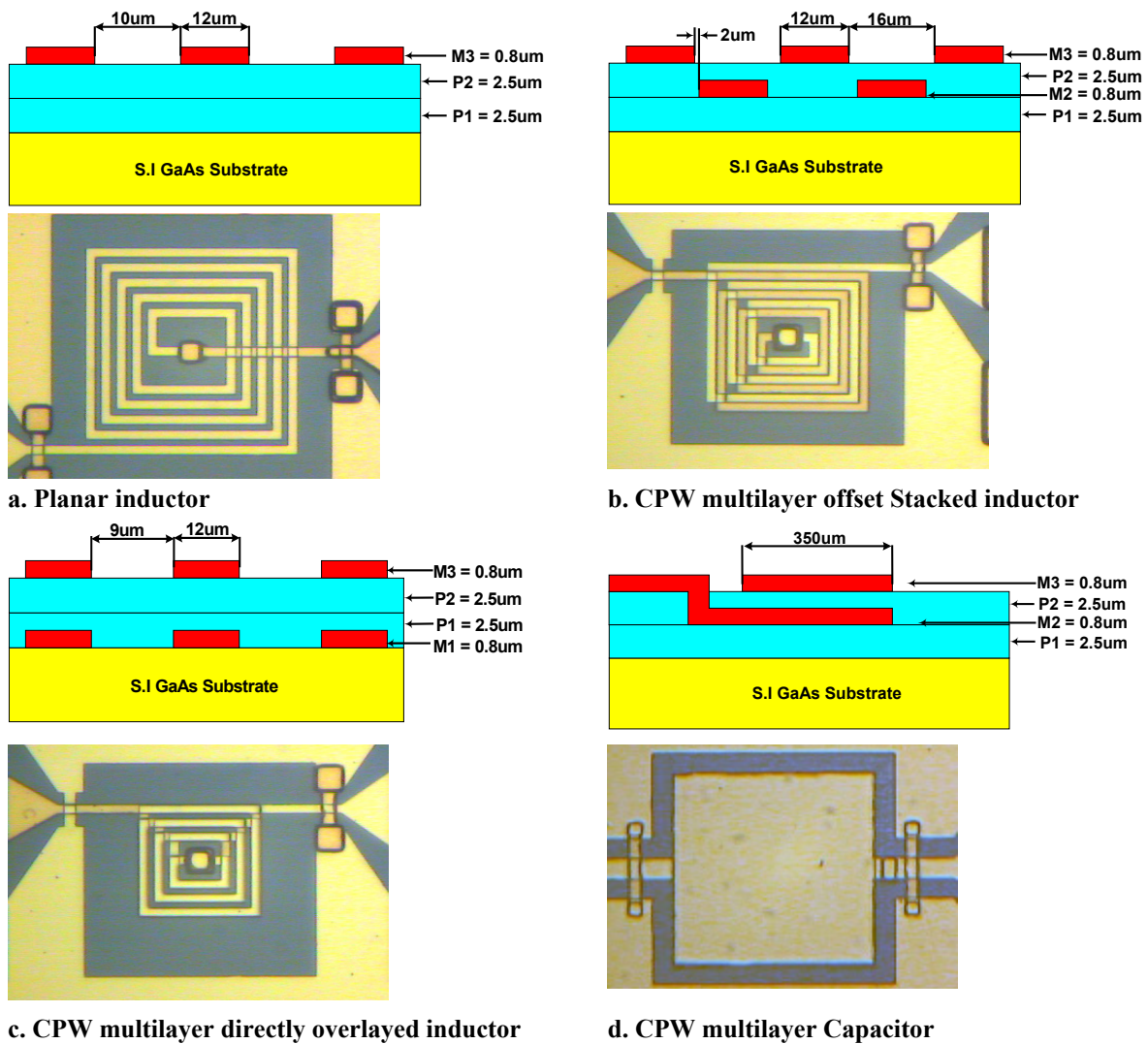


Fig. 1. Cross-sectional view and micrograph of the fabricated inductors and capacitors: a) Planar inductor 5.5 turns (M3), b) Offset stacked spirals 3+3 turns (M2-M3), c) Directly overlaid spirals 3+3 turns (M1-M3) and d) CPW capacitor

On the other hand the CPW multilayer capacitors can easily be used in MMICs, which saves area and reduce the parasitics. In this work CPW multilayer capacitors with different areas are designed, fabricated and tested utilizing the multilayer technology developed during this project.

From the variations of capacitance with area one can deduce a dielectric constant of 3.9 (figure 2), which is close to the manufacturers data.

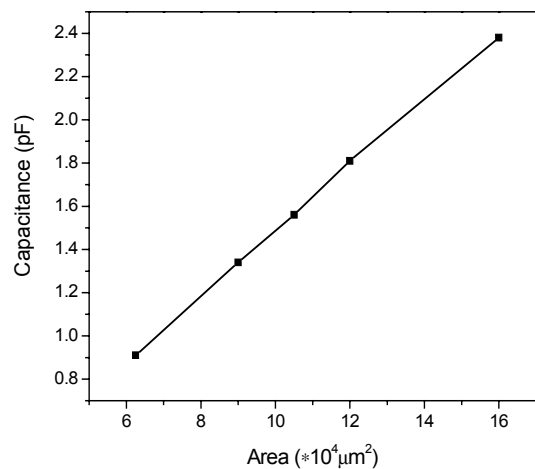


Fig.2. Variation of capacitance with area at room temperature (measured at 1 MHz)

Multilayer Inductors

In this work the multilayer inductors have been fabricated using three layers of metals and two layers of polyimide. Three types inductors have been studied: planar, offset and directly overlaid inductors. The equations used in the design and analysis of the inductors is given in [2]. For planar inductors the total inductance, L_s is given by:

$$L_s = L_0 + M^+ - M^- \quad (1)$$

Where, L_0 is the self-inductance, M^+ and M^- is the positive and negative mutual inductances respectively. To determine L_0 , M^+ and M^- we have used the following equations [2]:

$$L_0 = \frac{\mu_0}{2\pi} l_T \left(\ln \frac{l_T}{n(w+t)} - 0.2 \right) \quad (2)$$

$$M^- = 0.47 \frac{\mu_0}{2\pi} l_T n \quad (3)$$

$$M^+ = \frac{\mu_0}{2\pi} l_T (n-1) \left[\begin{array}{l} \ln \left(\sqrt{1 + \left(\frac{l_T}{4nd} \right)^2} + \frac{l_T}{4nd} \right) \\ - \sqrt{1 + \left(\frac{4nd}{l_T} \right)^2} + \frac{4nd}{l_T} \end{array} \right] \quad (4)$$

where d is the average distance of all segments given by:

$$d = (w+s) \left(\frac{\sum_{i=1}^{(n-i)>0} i(n-i)}{\sum_{i=1}^{(n-i)>0} (n-i)} \right) \quad (5)$$

μ_0 is the permeability, l_T is the total length of the conductor, w is the width of the conductor, t is the thickness of the conductor, n is the number of turns, s is the gap between the two conductors.

For multilayer inductors the total inductance $L_{stacked}$ is given in [3]:

$$L_{stacked} = 4L_{spiral} - 2L_{microstrip} \quad (6)$$

where, L_{spiral} is the inductance of the spiral inductor and $L_{microstrip}$ is the self-inductance of the unwound spiral inductor.

The parameters of interest in an inductor are its resonant frequency (f_{res}) and the Q factor. The resonant frequency is the frequency where the capacitive and

inductive reactance becomes equal hence the imaginary of Z_{in} becomes zero. The f_{res} and Q of the inductors are expected to be as high as possible as these are the two main limiting factors of their applications in MMIC circuits. The resonant frequency is dependent on the parasitic capacitance associated with the inductor. In order to reduce the capacitance in multilayer inductors the spirals are placed on different layers with a dielectric layer of $5\mu\text{m}$ thick. In offset stacked inductors the parasitic capacitance is further reduced due to the additional offset given between the layers.

The Q factor of an inductor can be defined as the ratio of the power stored to the dissipated power. The Q factor is dependent on the temperature and therefore a detailed investigation is required to study the variation of Q with temperature. The Q factor can be represented in terms of real and imaginary parts of the input impedance of an inductor and is given by:

$$Q = \frac{X_L}{R} = \frac{\text{Im}(Z_{in})}{\text{Re}(Z_{in})} = \frac{\text{Im} \left(\frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} \right)}{\text{Re} \left(\frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} \right)} \quad (7)$$

where the reflection co-efficient Γ_{in} is

$$\Gamma_{in} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}} \quad (8)$$

Table 1 is the summary of the fabricated inductor parameters extracted and those of the calculated using expressions (1-5).

TABLE 1: Inductor parameters at room temperature

Inductors design	No. of turns	Cal. L (nH)	Meas. L (nH)	f_{res} (GHz)
Planar (M3)	5.5	7.3	6.9	5.7
Offset stacked (M2-M3)	3+3	4.7	4.5	6.3
Offset stacked (M1-M3)	3+3	4.7	4.6	6.6
Directly Overlay (M1-M3)	3+3	3.9	3.7	7.2

Experimental results and discussion

On-wafer measurements are carried out using HP8510C Network Analyser and Cascade Microtech probe station to control the temperature from -25 to 200°C over a wide range of frequency from 45 MHz to 40 GHz. LRRM calibration is used to calibrate the Network Analyzer. To extract the parameters Agilent technologies ADS2003C simulation software is employed.

Electrical Performance of Multilayer Capacitors

The equivalent circuit used to extract the parameters of multilayer capacitor is shown in figure 3.

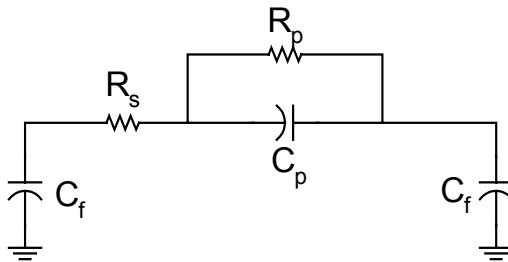


Fig. 3. Equivalent circuit of CPW multilayer capacitor

When CPW multilayer capacitors are analysed over temperature and frequency the capacitance remained almost constant with a minor variation of 3 to 5% as shown in figure 4. This type of thermal stability of the multilayer capacitors makes it more attractive for the MMIC applications. The multilayer capacitors realized have a Q value, which varies with temperature from 80 to 140 as shown in figure 5. The decrease in the Q at room temperature is due to moisture present in the dielectric material. The Q increases with increase in temperature due to increase in the parallel resistor R_p as can be estimated by:

$$Q = 2\pi f C_p R_p \quad (9)$$

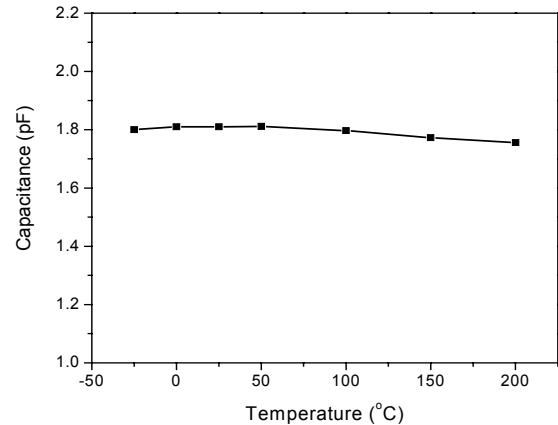


Fig. 4. Capacitance variation with temperature ($350 \times 350 \mu\text{m}^2$)

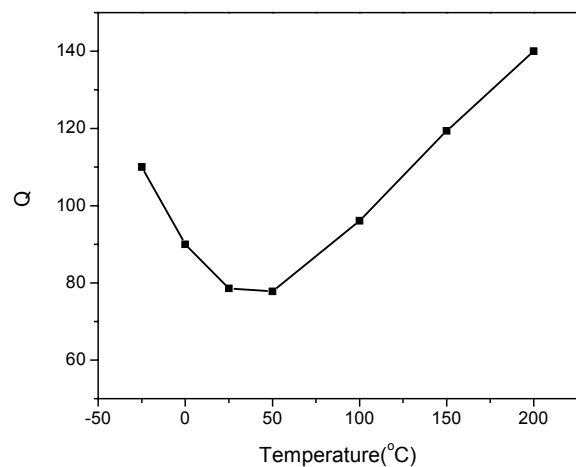


Fig. 5. Q factor variation of multilayer capacitor with temperature at 1MHz ($350 \times 350 \mu\text{m}^2$)

Electrical Performance of Planar and Multilayer Inductors

The equivalent circuit used to extract different parameters of an inductor is shown in figure 6. The inductance over temperature for a 5.5 turn planar and 3+3 turn multilayer inductors (both offset and directly overlaid inductors) is shown in figure 7. It is observed that the inductance varies only by 2 to 4% over the entire temperature range while the resonant frequency (figure 8) remains constant as expected.

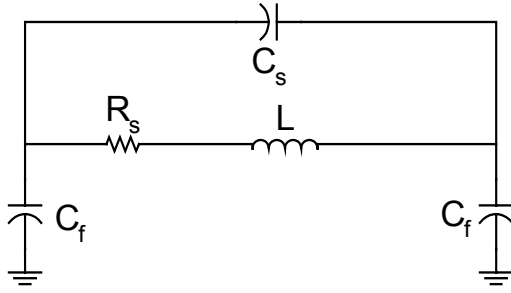


Fig. 6. Equivalent circuit of CPW multilayer inductor

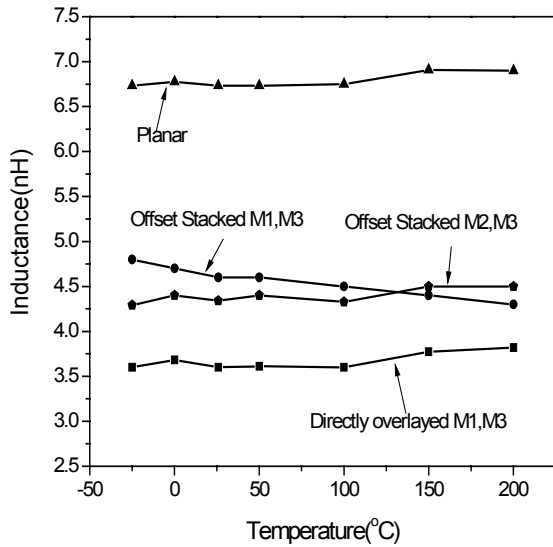


Fig. 7. Variation of inductances with temperature for planar (5.5 turns) and multilayer (3+3 turns) inductors over temperature

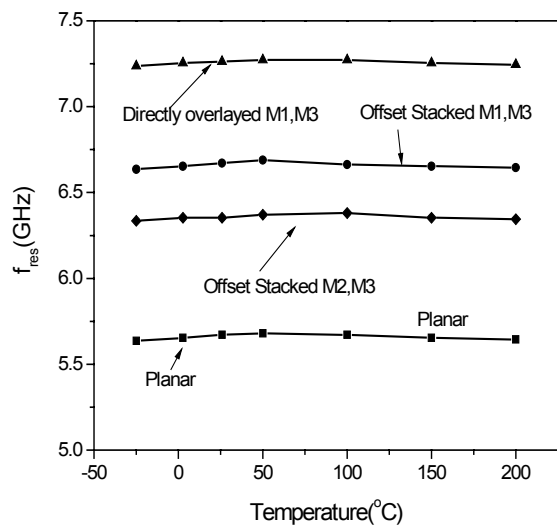


Fig. 8. Variation of resonant frequency planar (5.5 turns) and multilayer (3+3 turns) inductors with temperature

The Q of an inductor is defined as the ratio of energy stored to the energy dissipated. The loss component of an inductor is a complex element, which is dependent on both temperature and frequency. The total loss in an inductor is the sum of DC series resistance loss, AC resistance loss due to skin effect and the loss due to eddy currents (increases with frequency). Gold is used as a conducting metal and a thin layer of titanium (15nm) is used to get better adhesion to GaAs. The resistance of gold dominates the total resistance of the inductor, as the thickness of gold (0.8µm) is much higher than the titanium.

The resistivity of any metal is temperature dependent and increases with temperature. The resistivity of a metal is given in [4].

$$\rho = \frac{(3K_B m T)^{\frac{1}{2}}}{n \lambda e^2} \quad (10)$$

where,
 K_B = Boltzmann constant
 m = mass of the electron
 T = absolute temperature
 n = density of the electrons
 λ = electron mean free path
 e = unit charge

The resistance R is related to ρ , length l and its area A

$$R = \rho \frac{l}{A} \quad (11)$$

From equations 7, 10 and 11 it is clear that the Q factor of an inductor decreases as the temperature increases. Using expressions (10) and (11) the variation of resistivity of gold and titanium with respect to temperature has been analysed and these are given in figure 9. Figure 10 shows the variation of Q normalized to length with temperature for both planar and multilayer inductors. While Q of a planar inductor changes by 40%, the multilayer Q changes only by 20 to 27% (from room temperature to 200°C). This is due to the shorter length of metal strip required in the realization of the inductor to achieve the same inductance, Q and resonant frequency.

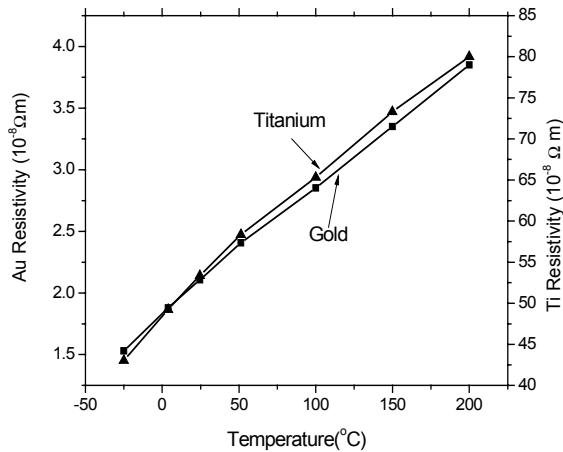


Fig. 9. Calculated variation of resistivity of gold and titanium with temperature

Inductors characterized in this work has a thin gold metal of about 0.8 μm . this metal layer can be increased to several micrometers in order to reduce the dissipation loss and hence achieve much higher Q values.

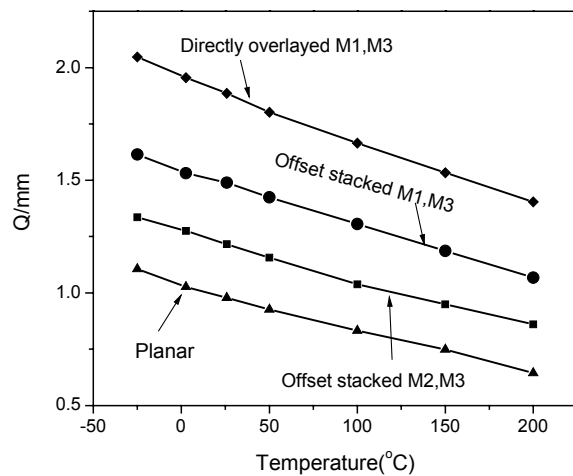


Fig. 10. Variation of Q factor with temperature for planar (5.5 turns) and multilayer (3+3 turns) inductors

Conclusion

In this work CPW multilayer capacitors and inductors are designed, fabricated and characterized over temperature and frequency. The inductance and capacitance of these components are observed to remain constant with temperature. A good agreement is obtained between the

calculated and the extracted values providing useful analysis for their applications in MMIC circuits. Q of an inductor determines the bandwidth of a circuit and we have shown that by using the multilayer techniques one can reduce the variation of Q with temperature. We therefore illustrated the advantages of using CPW multilayer technology in developing advanced MMICs.

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