PHEMT FREQUENCY DIVIDERS

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ABSTRACT

The principles of subharmonic generation using a nonlinear reactance can be used and applied to an active semiconductor device such as a Pseudomorphic High Electron Mobility Transistor (PHEMT). This project aims to provide an active analogue parametric frequency divider using the input nonlinear junction capacitance of PHEMTs. The objective is to achieve higher conversion efficiencies and easier cascadability for higher order division ratios. This paper gives an overview of the proposed research and outlines the principle theory behind the research idea and a brief description of work completed so far.

Keywords: frequency dividers, parametric PHEMT dividers, nonlinear subharmonic generation

INTRODUCTION

Nowadays, communication systems require sophisticated frequency generation circuits in which frequency synthesizers play an important role. Frequency division is a key function of those circuits.

Frequency dividers find applications in many different systems from low-cost theft prevention systems [1] to military applications. They are also essential to a variety of communications system needs. Among the classic examples are applications involving straight frequency counting and phase-locked loops.

Frequency division is a frequency conversion process similar to heterodyning. The Heterodyne technique relies on mixing a signal from a local oscillator with the microwave input signal. During this conversion, the absolute bandwidth remains unchanged and the fractional bandwidth increases. Unlike the heterodyne technique frequency divider circuits reduce the absolute bandwidth in the division process by dividing each frequency component in the input band by a constant amount, and thus preserving the fractional bandwidth. Frequency dividers therefore have bandwidth compression capabilities which opens up the possibility of transferring wide microwave bands, while retaining accurate frequency and phase information, to the region where the power of digital logic can be used for processing [2].

Frequency division can be performed in a digital or an analog way. Digital dividers are capable of broadband performances up into the microwave frequency range (up to 40 GHz) but also exhibit excessive power consumption (several watts DC power) at millimetre wavelengths. Analogue dividers feature lower power consumption, simpler circuit designs and higher operating frequencies, which makes them attractive for communications purposes.

Among the various analogue solutions [3], parametric frequency dividers [4-5], represent simpler circuit configuration and broader synchronisation bandwidth. Parametric division is to some extent a less common process, in which a subharmonic oscillation is generated from a nonlinear reactive element. The most common element used in these dividers is a varactor i.e. the nonlinear capacitance of an abrupt junction diode. The basic theory of device operation is presented in [6] and [7].

Divider designs based on the empirical techniques are described in [8-10].

Because of circuit losses within the varactor diodes, amplifiers are generally required to recover the input signal level. For systems that require cascaded frequency dividers at least one amplifier is required for each frequency divider. The proposed active parametric frequency divider design eliminates the need for separate amplifiers. The design employs a PHEMT device to perform parametric frequency division and amplification simultaneously at microwave frequencies.

This aim of this project is to develop working designs for an active parametric frequency divider and to eventually fabricate the circuit configurations in MMIC form. Once designed, fabricated and tested, the performance will be evaluated and compared with theoretical predictions and also other major types of dividers. This research project is still ongoing and is expected to be finished by 2006.

PARAMETRIC DIVIDER THEORY

The name parametric has become associated with a class of amplifying and frequency-converting devices which utilize the properties of nonlinear or time-varying reactances. These reactances channel energy from an ac source to a useful load and are capable of power conversion from one frequency to another.

Manley and Rowe [11] have derived a general set of equations relating power flowing into and out of an ideal nonlinear reactance with no specific nonlinearity specified. It uses the principle of energy conservation and can be used to show the possibility of frequency division [7].

The basic theory of active (PHEMT) frequency dividers is similar to nonlinear reactance frequency dividers. Figure 1 shows the diagram of a simple parametric frequency divider using a varactor (nonlinear voltage-dependant capacitor). For frequency division, the input and output coupling networks have to be properly adjusted. In this case, the coupling networks (i.e. filters) in their simplest form can consist of resonant LC networks tuned at the required input and output frequency. Theoretically if the varactor is ideal i.e. lossless and the filters are extremely selective (i.e. high Q), then it is possible to achieve very high efficiencies with this circuit.

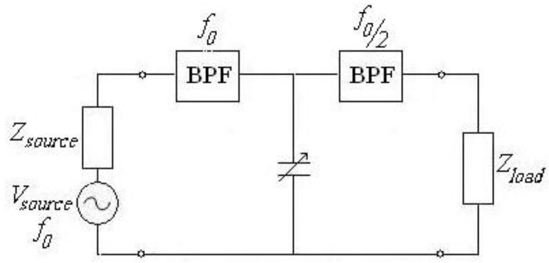


Figure 1 – Simple varactor parametric frequency divider circuit

Varactors, when pumped, generate power not only at harmonics but at subharmonics of the pumping frequency. In doing so, varactors behave much like oscillators: as the output current builds up, nonlinear effects reduce the rate of amplitude rise and finally a steady-state with a constant output power is reached [10].

For the analysis, we assume that the subharmonic current is present in the circuit in some form or another for it to grow in magnitude, rather like an oscillator. This assumption is valid since there is always some noise in the system. This is the essential difference between a frequency multiplier and a divider. Also in a frequency multiplier there will always be some harmonics present regardless of the magnitude of the input, but frequency dividers have a power threshold level below which subharmonics cannot exist. This threshold level is the power required to overcome the losses in the output circuit for subharmonic oscillations to occur. This is the fundamental difference between a frequency divider and subharmonic oscillator.

The principles of a nonlinear reactance frequency divider can be used and applied to an active semiconductor device such as a PHEMT. The input nonlinear junction capacitance in a PHEMT, used with similar input and output matching networks, functions as a varactor divider producing subharmonics and the device transconductance g_m simultaneously provides amplification.
The semi-unilateral property of active devices provides excellent isolation between resonant input and output loops. It means that the output will not necessarily see the same impedance as the input. This implies that in order for frequency division to take place, all the input and output matching circuitry has to be on the input side of the PHEMT (Figure 2). So the required subharmonic current is generated in the input side and amplified by the controlled current source. A highly selective bandpass filter at the output selects the required output subharmonic frequency. So the output signal is amplified as well as divided in frequency.

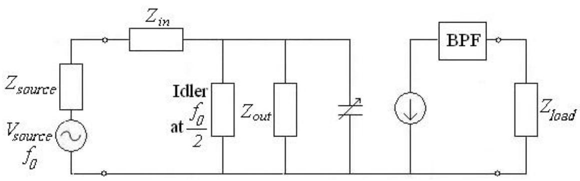


Figure 2 – simplified model of the parametric PHEMT frequency divider

To obtain higher order 2^N division we can cascade several dividers. The associated gain of the nonlinearity used to achieve frequency division, compensates for most of the conversion losses. This fact enables more frequency dividers to be cascaded without worrying too much about signal degradation and power loss.

SIMULATION AND DESIGN

Since frequency dividers are, by nature, potentially unstable i.e. are very sensitive to mismatches and may produce spurious oscillations, the ability to predict the overall circuit behaviour and performances by computer simulation is important [12].

While frequency-domain techniques remain the basis for most RF/microwave design, time-domain simulation can provide an important complement and a more natural solution to study analogue frequency dividers. The softwares being used are Advanced Design Systems (ADS) from Agilent, and MATLAB and Simulink from MathWorks.
As part of the project's initial aims, to model and simulate different types of frequency divider circuits, general regenerative and injection-locked frequency divider circuits were successfully simulated in ADS. Since the PHEMT divider uses the principles of nonlinear reactance subharmonic generation, more time was spent on understanding and modelling a varactor frequency divider circuit, in particular to correctly model the nonlinear capacitance.

The nonlinear voltage-dependent capacitor (or varactor) was modelled using a Symbolically Defined Device (SDD) inside ADS and a model created for the biased varactor with a series resistor and inductor and a shunt capacitor as the parasitics of the real device. The simulated results from this equivalent model were compared with experimental measurements of varactor diodes and since they showed good harmony, the model was inserted into a parametric frequency divider circuit similar to the circuit shown in Figure 1. The circuit produced frequency division with certain circuit parameters and settings. However the transient simulator has convergence problems and does not allow the complete simulation of the circuit. This is being investigated further to optimise the transient simulator options to best match the output requirements.

In addition to ADS which is a specialised simulation software for microwave circuits, MATLAB and Simulink can also be used for modelling, simulating, and analyzing dynamic systems. This approach gives confidence in the exact behaviour of the circuit model as it numerically solves the circuit equations.

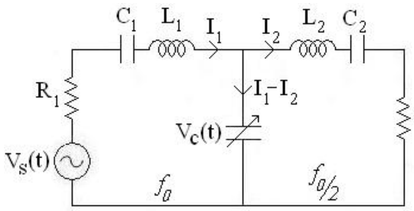


Figure 3 – Simple lumped element circuit of the varactor frequency divider

Figure 3 shows the simple varactor frequency divider in lumped element form i.e. with LRC networks in the input and output loops. The circuit basically consists of the shunt varactor nested between two resonant LC circuits (filters). The input LC network is tuned to the input frequency and allows the pump energy to reach the varactor, and it isolates the source impedance, R_1, from the subharmonic oscillations occurring at the diode. The output LC network is tuned to the subharmonic frequency. At the pump frequency this filter prevents the pump energy from reaching the load impedance, R_2.

Two relationships can be written for the circuit in terms of the input and output loops as follows:

$$V_s(t) = V_1(t) + V_c(t)$$
$$= i_1 R_1 + L_1 \frac{di_1}{dt} + \frac{1}{C_1}\int i_1 dt + V_c(t) \qquad (1)$$

$$V_c(t) = V_2(t)$$
$$= i_2 R_2 + L_2 \frac{di_2}{dt} + \frac{1}{C_2}\int i_2 dt \qquad (2)$$

where $V_1(t)$ and $V_2(t)$ are the voltages across the input and output RLC networks respectively. Also the voltage across the varactor can be expressed as

$$V_c(t) = \Phi - m(q(t) - q_\Phi)^2 \qquad (3)$$

Since

$$C = \frac{dq}{dv} = \frac{C_{j0}}{\left(1 - \frac{v}{\Phi}\right)^{1/2}} \qquad (4)$$

where $m = \frac{1}{4C_{j0}{}^2\Phi}$

C_{j0} = zero-voltage junction capacitance

Φ = junction in-built potential

q_Φ = charge at v = Φ

$q(t)$ = instantaneous charge on the varactor

v = instantaneous voltage across varactor

With a few rearrangements and substitutions, the above circuit equations can be converted into the block diagram model below (Figure 4), where each block represents a mathematical operation or function. The model is then simulated to solve the relationships numerically and the MATLAB graphical interface is used to display the outputs.

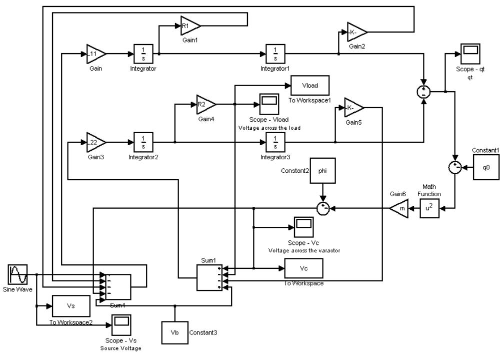


Figure 4 – Simulink block diagram model of the simple varactor frequency divider.

The circuit was simulated with different input values and the results clearly showed frequency division at particular power levels (Figure 5). It also demonstrated the existence of the threshold level in the divider operation. Figure 6 shows the extracted threshold and frequency range for a 1 – 0.5 GHz divider circuit.

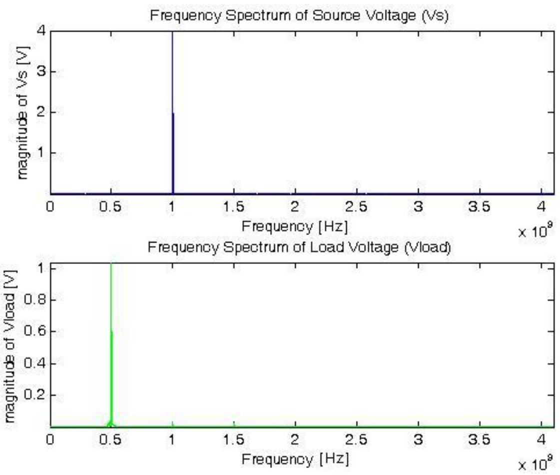
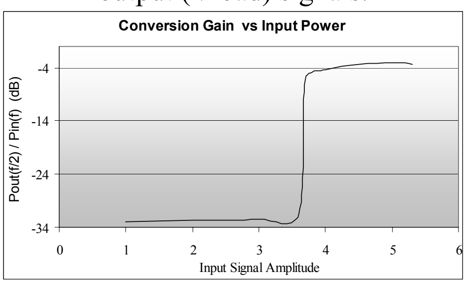
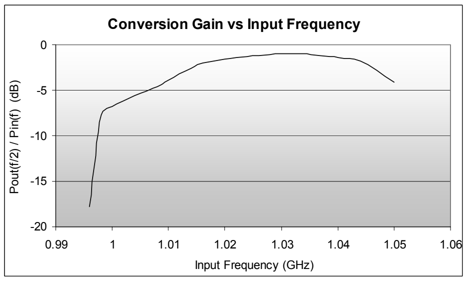


Figure 5 – MATLAB simulation results of the frequency spectrum of the Input (Vs) and output (Vload) signals.



(a)



(b)

Figure 6 - (a) Simulink simulation results showing input signal threshold level and (b) working frequency range.

The Simulink model has also been modified to include the simple PHEMT divider circuit. However, the simulations for this are still ongoing to determine more optimised results and be able to model the practical circuit more accurately.

PRACTICAL ACHIEVEMENTS

A prototype PHEMT divider at 1GHz is under construction using a mixture of lumped elements and transmission lines. The filter circuits have to be designed to have as high Q as possible with low loss, which is being investigated at that frequency. Also, in order to have a better idea of the nonlinear capacitance–voltage relationships of a PHEMT, some measurements were taken of the LP1500 PHEMT from Filtronic. These would help in the better understanding and modelling of the device.

CONCLUSIONS AND FUTURE PLANS

An account of the proposed active parametric frequency divider using PHEMTs has been made and an overview of the parametric divider theory has been presented. Also a brief description of work completed so far has been given.

The main objective of the project is to design and build an active parametric divider using PHEMTs, implemented in MMIC form. It can then be compared with other designs such as a regenerative PHEMT divider.

Low-frequency prototype PHEMT divider will be built and tested. The simulation investigations continue until a complete design that fully models the circuit functionality is achieved. The intention is then to proceed to MMIC circuit designs.

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